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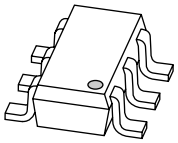


# PBSS5440D

## 40 V PNP low $V_{CEsat}$ (BISS) transistor

**Rev. 02 — 14 December 2009** **Product data sheet**

## 1. Product profile

### 1.1 General description

PNP low $V_{CEsat}$ Breakthrough in Small Signal (BISS) single bipolar PNP transistor in a SOT457 (SC-74) SMD plastic package.

NPN complement: PBSS4440D.

### 1.2 Features

- Ultra low collector-emitter saturation voltage $V_{CEsat}$
- 4 A continuous collector current capability $I_C$ (DC)
- Up to 15 A peak current
- Very low collector-emitter saturation resistance
- High efficiency due to less heat generation

### 1.3 Applications

- Power management functions
- Charging circuits
- DC-to-DC conversion
- MOSFET gate driving
- Power switches (e.g. motors, fans)
- Thin Film Transistor (TFT) backlight inverter

### 1.4 Quick reference data

**Table 1. Quick reference data**

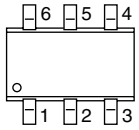
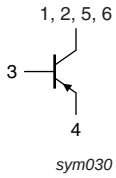
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CEO}$ | collector-emitter voltage | open base | | - | - | −40 | V |
| $I_C$ | collector current (DC) | | [1] | - | - | −4 | A |
| $I_{CM}$ | peak collector current | t = 1 ms or limited by $T_{j(max)}$ | | - | - | −15 | A |
| $R_{CEsat}$ | collector-emitter saturation resistance | $I_C$ = −6 A; $I_B$ = −600 mA | [2] | - | 55 | 75 | mΩ |

[1] Device mounted on a ceramic Printed-Circuit Board (PCB), $AL_2O_3$, standard footprint.

[2] Pulse test: $t_p \leq 300\ \mu s$; $\delta \leq 0.02$.

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | collector |  |  |
| 2 | collector | | |
| 3 | base | | |
| 4 | emitter | | |
| 5 | collector | | |
| 6 | collector | | |



## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PBSS5440D | SC-74 | plastic surface mounted package; 6 leads | SOT457 |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PBSS5440D | 71 |

## 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CBO}$ | collector-base voltage | open emitter | | - | –40 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | –40 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | | - | –5 | V |
| $I_C$ | collector current (DC) | | [1] | - | –4 | A |
| $I_{CM}$ | peak collector current | t = 1 ms or limited by $T_{j(max)}$ | | - | –15 | A |
| $I_B$ | base current (DC) | | | - | –0.8 | A |
| $I_{BM}$ | peak base current | $t_p \leq 300$ µs | | - | –2 | A |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [2] | - | 360 | mW |
| | | | [3] | - | 600 | mW |
| | | | [4] | - | 750 | mW |
| | | | [1] | - | 1.1 | W |
| | | | [2][5] | - | 2.5 | W |

**Table 5. Limiting values** *…continued*

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |
| $T_j$ | junction temperature | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | −65 | +150 | °C |

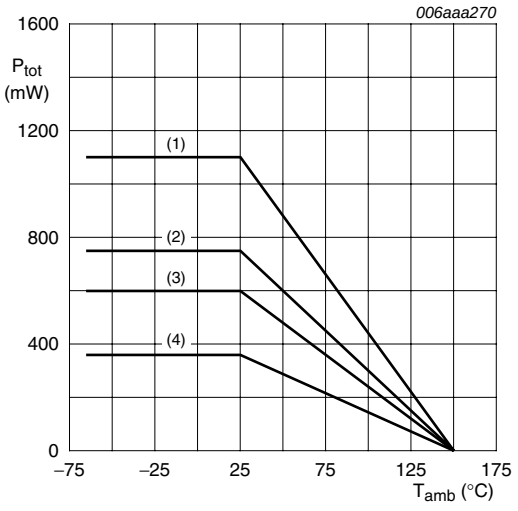
[1] Device mounted on a ceramic PCB, $AL_2O_3$, standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 $cm^2$.

[4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 $cm^2$.

[5] Operated under pulsed conditions: Duty cycle $\delta \leq 10\%$ and pulse width $t_p \leq 10$ ms.




(1) Ceramic PCB, $AL_2O_3$, standard footprint

(2) FR4 PCB, mounting pad for collector 6 $cm^2$

(3) FR4 PCB, mounting pad for collector 1 $cm^2$

(4) FR4 PCB, standard footprint

**Fig 1. Power derating curves**

## 6. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 350 | K/W |
| | | | [2] | - | - | 208 | K/W |
| | | | [3] | - | - | 160 | K/W |
| | | | [4] | - | - | 113 | K/W |
| | | | [1][5] | - | - | 50 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | - | 45 | K/W |

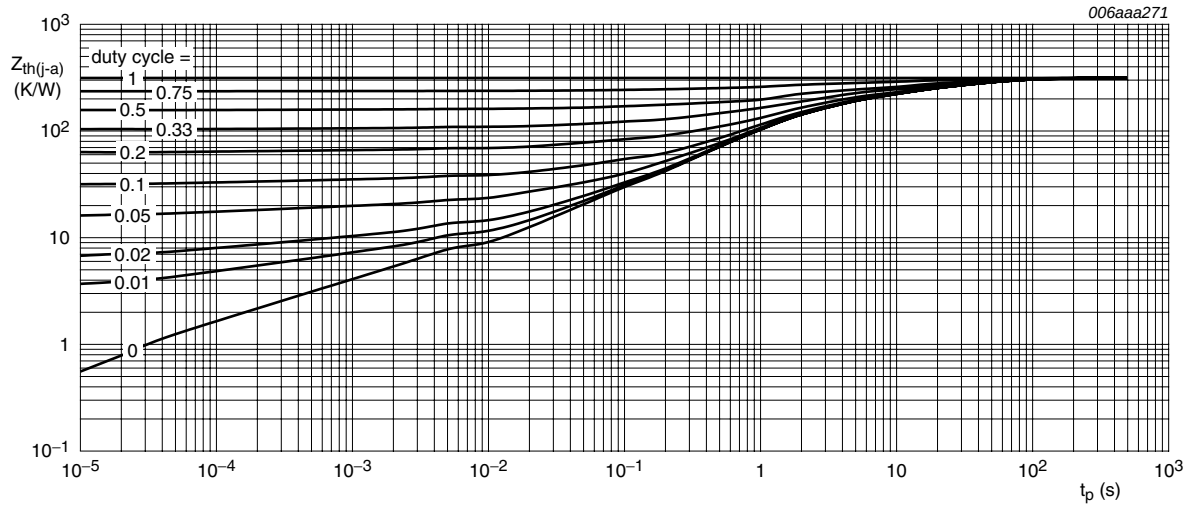
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 $cm^2$.

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 $cm^2$.

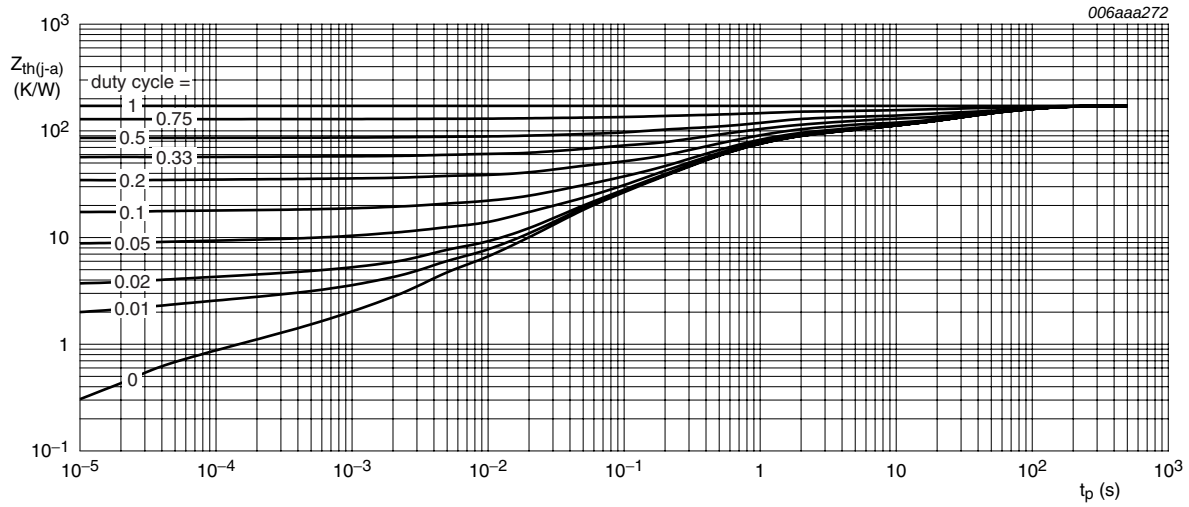
[4] Device mounted on a ceramic PCB, $AL_2O_3$, standard footprint.

[5] Operated under pulsed conditions: Duty cycle $\delta \leq 10\%$ and pulse width $t_p \leq 10$ ms.



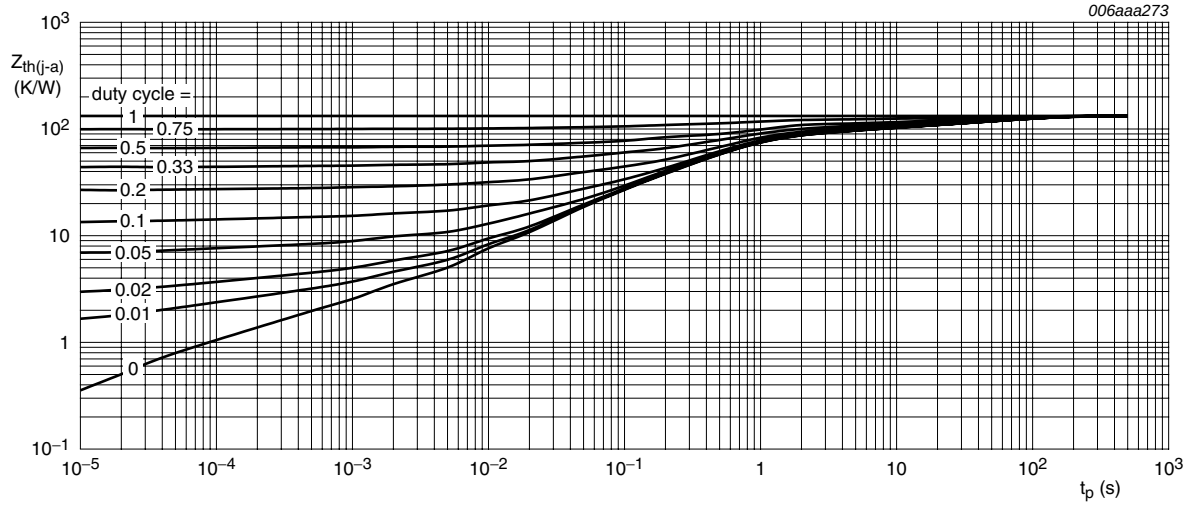

FR4 PCB, standard footprint

**Fig 2. Transient thermal impedance from junction to ambient as a function of pulse time; typical values**




FR4 PCB, mounting pad for collector 1 $cm^2$

**Fig 3. Transient thermal impedance from junction to ambient as a function of pulse time; typical values**




FR4 PCB, mounting pad for collector 6 $cm^2$

**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse time; typical values**

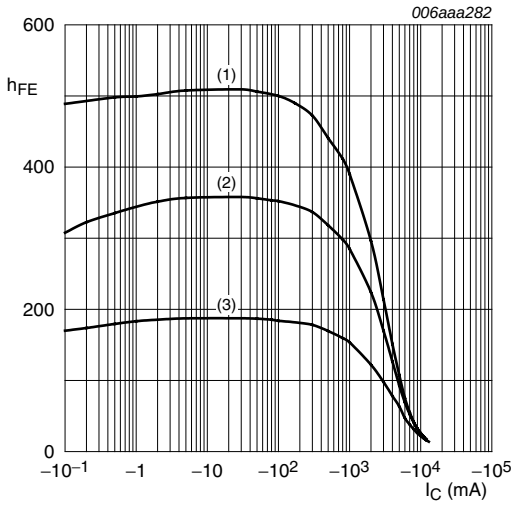
# 7. Characteristics

**Table 7. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = –30 V; $I_E$ = 0 A | | - | - | –0.1 | µA |
| | | $V_{CB}$ = –30 V; $I_E$ = 0 A; $T_j$ = 150 °C | | - | - | –50 | µA |
| $I_{CES}$ | collector-emitter cut-off current | $V_{CE}$ = –30 V; $V_{BE}$ = 0 V | | - | - | –0.1 | µA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = –5 V; $I_C$ = 0 A | | - | - | –0.1 | µA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = –2 V; $I_C$ = –0.5 A | | 200 | - | - | |
| | | $V_{CE}$ = –2 V; $I_C$ = –1 A | [1] | 200 | - | - | |
| | | $V_{CE}$ = –2 V; $I_C$ = –2 A | [1] | 175 | - | - | |
| | | $V_{CE}$ = –2 V; $I_C$ = –4 A | [1] | 80 | - | - | |
| | | $V_{CE}$ = –2 V; $I_C$ = –6 A | [1] | 30 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = –0.5 A; $I_B$ = –50 mA | | - | –46 | –60 | mV |
| | | $I_C$ = –1 A; $I_B$ = –50 mA | | - | –70 | –110 | mV |
| | | $I_C$ = –2 A; $I_B$ = –200 mA | | - | –120 | –180 | mV |
| | | $I_C$ = –4 A; $I_B$ = –400 mA | [1] | - | –220 | –300 | mV |
| | | $I_C$ = –6 A; $I_B$ = –600 mA | [1] | - | –320 | –450 | mV |
| $R_{CEsat}$ | collector-emitter saturation resistance | $I_C$ = –6 A; $I_B$ = –600 mA | [1] | - | 55 | 75 | mΩ |
| $V_{BEsat}$ | base-emitter saturation voltage | $I_C$ = –0.5 A; $I_B$ = –50 mA | | - | –0.8 | –0.85 | V |
| | | $I_C$ = –1 A; $I_B$ = –50 mA | | - | –0.84 | –0.9 | V |
| | | $I_C$ = –1 A; $I_B$ = –100 mA | [1] | - | –0.84 | –1 | V |
| | | $I_C$ = –4 A; $I_B$ = –400 mA | [1] | - | –1.0 | –1.1 | V |
| $V_{BEon}$ | base-emitter turn-on voltage | $V_{CE}$ = –2 V; $I_C$ = –2 A | | - | –0.8 | –1.0 | V |
| $t_d$ | delay time | $V_{CC}$ = –10 V; $I_C$ = –2 A; $I_{Bon}$ = –0.1 A; $I_{Boff}$ = 0.1 A | | - | 12 | - | ns |
| $t_r$ | rise time | | | - | 43 | - | ns |
| $t_{on}$ | turn-on time | | | - | 55 | - | ns |
| $t_s$ | storage time | | | - | 240 | - | ns |
| $t_f$ | fall time | | | - | 80 | - | ns |
| $t_{off}$ | turn-off time | | | - | 320 | - | ns |
| $f_T$ | transition frequency | $V_{CE}$ = –10 V; $I_C$ = –0.1 A; f = 100 MHz | | - | 110 | - | MHz |
| $C_c$ | collector capacitance | $V_{CB}$ = –10 V; $I_E$ = $i_e$ = 0 A; f = 1 MHz | | - | 50 | - | pF |

[1] Pulse test: $t_p \leq 300$ µs; $\delta \leq 0.02$.



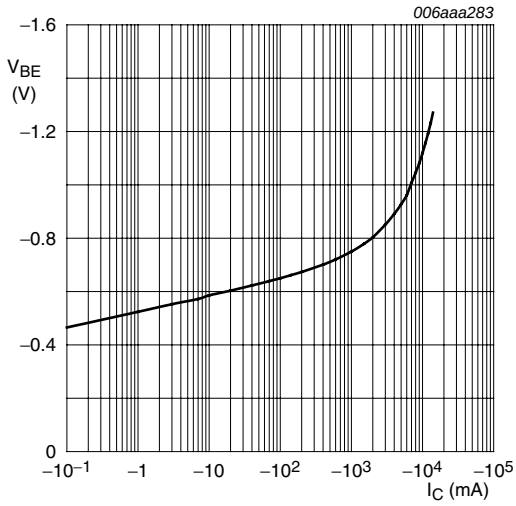

$V_{CE}$ = −2 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −55 °C

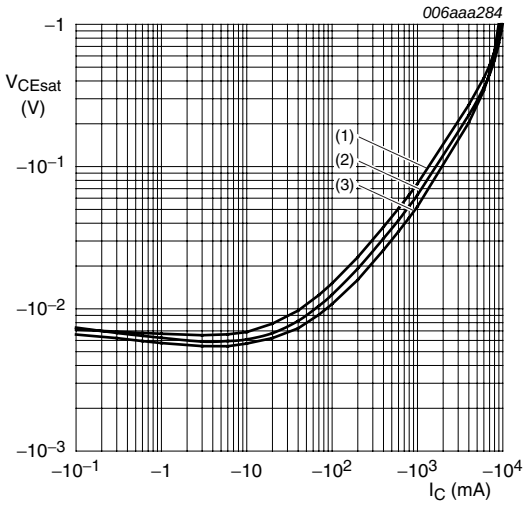
**Fig 5. DC current gain as a function of collector current; typical values**




$V_{CE}$ = −2 V

$T_{amb}$ = 25 °C

**Fig 6. Base-emitter voltage as a function of collector current; typical values**



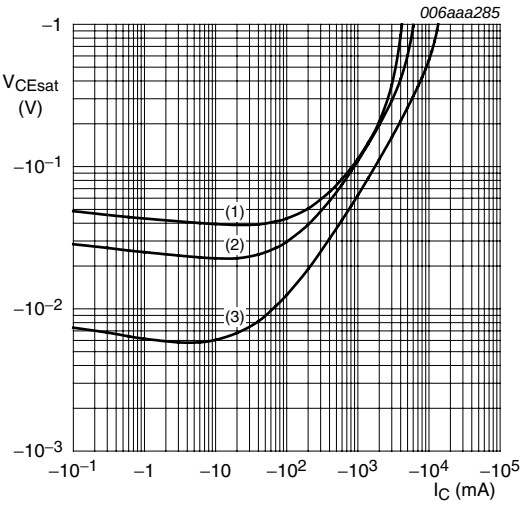

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −55 °C

**Fig 7. Collector-emitter saturation voltage as a function of collector current; typical values**



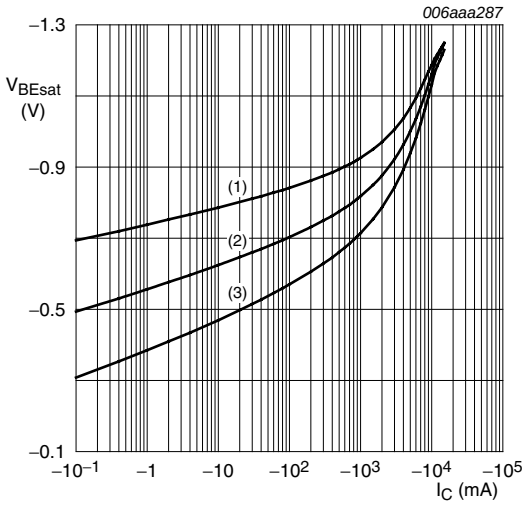

$T_{amb}$ = 25 °C

(1) $I_C/I_B$ = 100

(2) $I_C/I_B$ = 50

(3) $I_C/I_B$ = 10

**Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values**



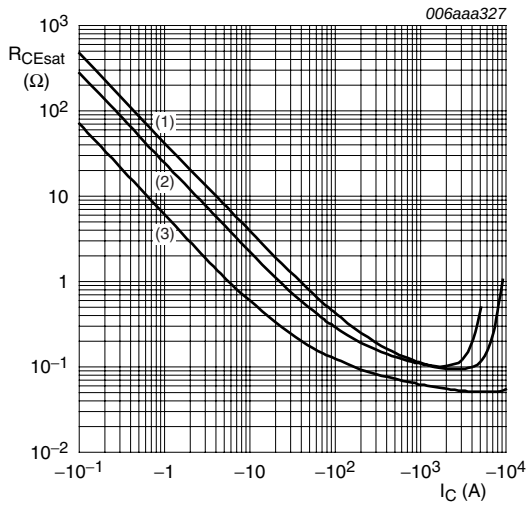

$I_C/I_B$ = 20

(1) $T_{amb}$ = −55 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 9. Base-emitter saturation voltage as a function of collector current; typical values**



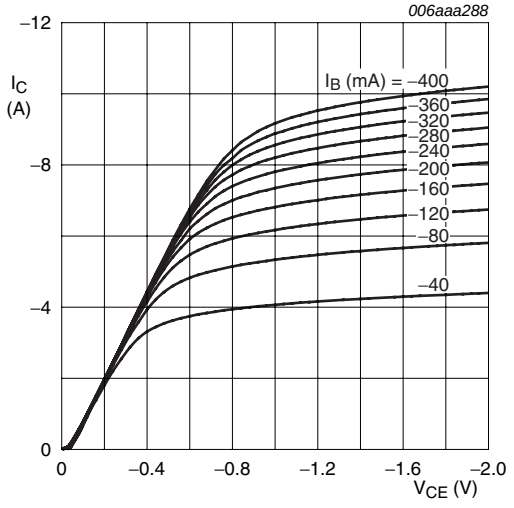

$T_{amb}$ = 25 °C

(1) $I_C/I_B$ = 100

(2) $I_C/I_B$ = 50

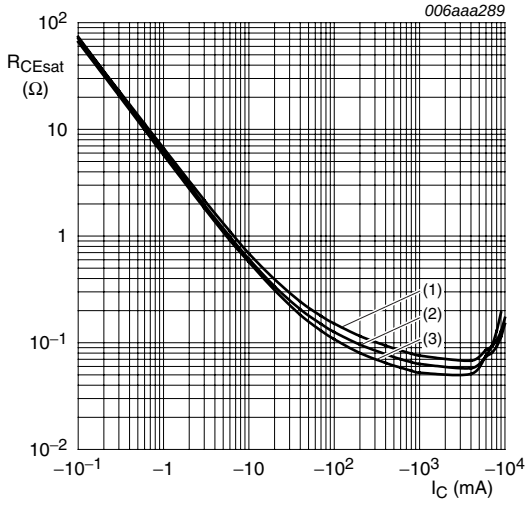
(3) $I_C/I_B$ = 10

**Fig 10. Collector-emitter saturation resistance as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 11. Collector current as a function of collector-emitter voltage; typical values**




$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −55 °C

**Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values**

## 8. Test information

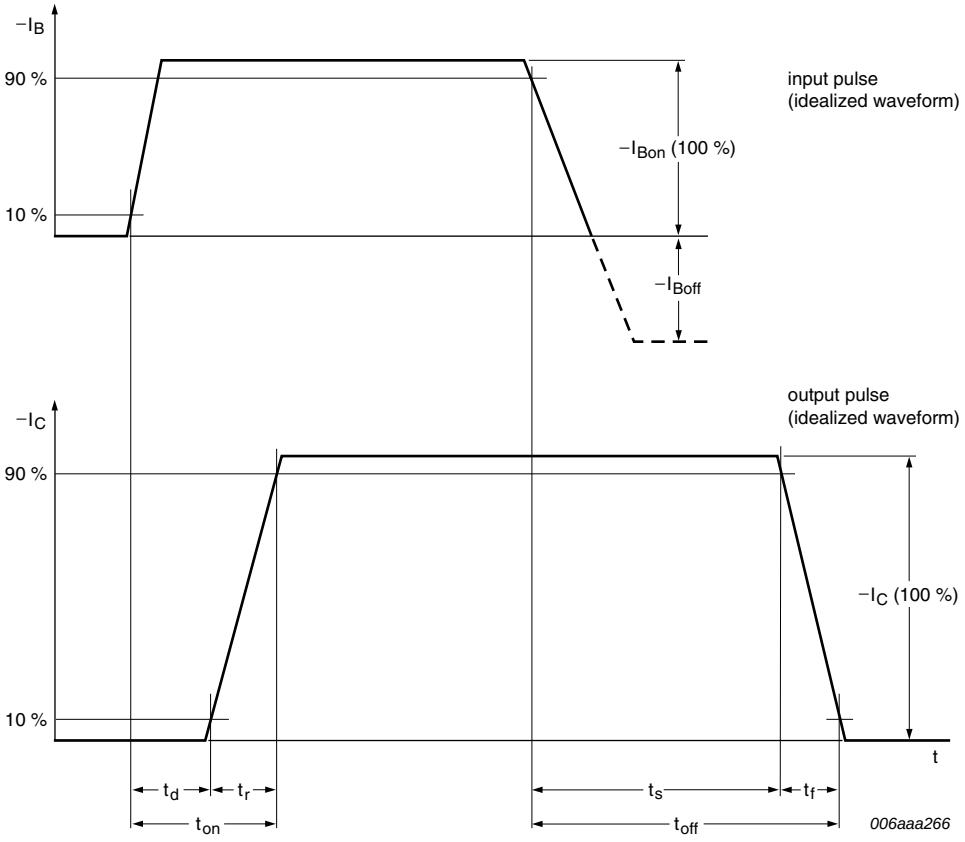
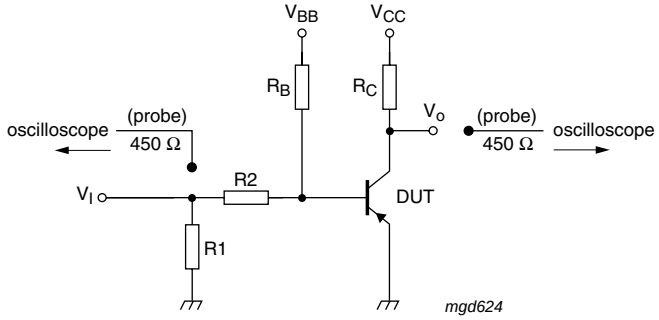



**Fig 13. BISS transistor switching time definition**




(1) $V_{CC}$ = −10 V; $I_C$ = −2 A; $I_{Bon}$ = −0.1 A; $I_{Boff}$ = 0.1 A

**Fig 14. Test circuit for switching times**

## 9. Package outline

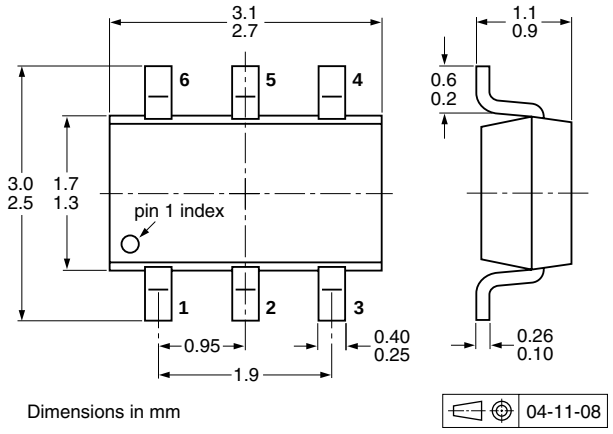



**Fig 15. Package outline SOT457 (SC-74)**

## 10. Packing information

**Table 8. Packing methods**

*The indicated -xxx are the last three digits of the 12NC ordering code.*[1]

| Type number | Package | Description | Packing quantity | | |
|---|---|---|---|---|---|
| | | | 3000 | 5000 | 10000 |
| PBSS5440D | SOT457 | 4 mm pitch, 8 mm tape and reel; T1 [2] | -115 | - | -135 |
| | | 4 mm pitch, 8 mm tape and reel; T2 [3] | -125 | - | -165 |

[1] For further information and the availability of packing methods, see Section 13.

[2] T1: normal taping

[3] T2: reverse taping

## 11. Revision history

**Table 9. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PBSS5440D_2 | 20091214 | Product data sheet | - | PBSS5440D_1 |
| Modifications: | • This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.<br>• Figure 2 “Transient thermal impedance from junction to ambient as a function of pulse time; typical values”: updated<br>• Figure 3 “Transient thermal impedance from junction to ambient as a function of pulse time; typical values”: updated<br>• Figure 4 “Transient thermal impedance from junction to ambient as a function of pulse time; typical values”: updated<br>• Figure 6 “Base-emitter voltage as a function of collector current; typical values”: updated<br>• Figure 11 “Collector current as a function of collector-emitter voltage; typical values”: updated | | | |
| PBSS5440D_1 | 20050427 | Product data sheet | - | - |

# 12. Legal information

## 12.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 14. Contents





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**Date of release: 14 December 2009**
**Document identifier: PBSS5440D_2**