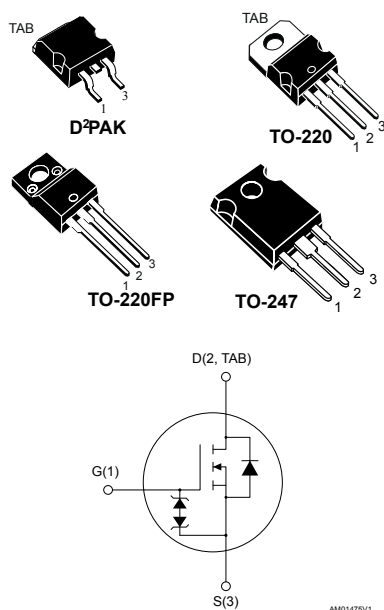


N-channel 900 V, 1.56 Ω typ., 5.8 A SuperMESH™ Power MOSFET in D²PAK, TO-220, TO-220FP and TO-247 packages



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STB6NK90ZT4	900 V	2 Ω	5.8 A
STP6NK90Z			
STP6NK90ZFP			
STW7NK90Z			

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status
STB6NK90ZT4
STP6NK90Z
STP6NK90ZFP
STW7NK90Z

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220, TO-247	TO-220FP	
V _{DS}	Drain-source voltage	900		V
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	5.8	5.8 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	3.65	3.65 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	23.2	23.2	A
P _{TOT}	Total dissipation at T _C = 25 °C	140	30	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	-	2500	V
T _J	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			°C

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. I_{SD} ≤ 5.8 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}.

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	TO-220	TO-220FP	TO-247	
R _{thj-case}	Thermal resistance junction-case	0.89		4.2	0.89	°C/W
R _{thj-pcb}	Thermal resistance junction-pcb	60				°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5			50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J Max)	5.8	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	300	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source	I _D = 1 mA, V _{GS} = 0 V	900			V
	Breakdown voltage					
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 900 V			1	μA
		V _{GS} = 0 V, V _{DS} = 900 V, T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2.9 A		1.56	2	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V		1350		pF
C _{oss}	Output capacitance			130		
C _{rss}	Reverse transfer capacitance			26		
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 V to 720 V		70		pF
t _{d(on)}	Turn-on delay time	V _{DD} = 450 V, I _D = 3 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 17. Test circuit for resistive load switching times and Figure 22. Switching time waveform)		17		ns
t _r	Rise time			20		
t _{r(off)}	Turn-off delay time			45		
t _f	Fall time			20		
Q _g	Total gate charge	V _{DD} = 720 V, I _D = 5.8 A, V _{GS} = 0 to 10 V (see Figure 18. Test circuit for gate charge behavior)		46.5	60.5	nC
Q _{gs}	Gate-source charge			8.5		
Q _{gd}	Gate-drain charge			25		
t _{r(Voff)}	Off-voltage rise time	V _{DD} = 720 V, I _D = 5.8 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 19. Test circuit for inductive load switching and diode recovery times)		11		ns
t _f	Fall time			12		
t _c	Cross-over time			20		

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				5.8	A
I_{SDM}	Source-drain current (pulsed)				23.2	
V_{SD}	Forward on voltage	$I_{SD} = 5.8 \text{ A}$, $V_{GS} = 0 \text{ V}$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 5.8 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		840		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 36 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)		5880		nC
I_{RRM}	Reverse recovery current			14		A

Table 7. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{gs} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	± 30			V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics curves

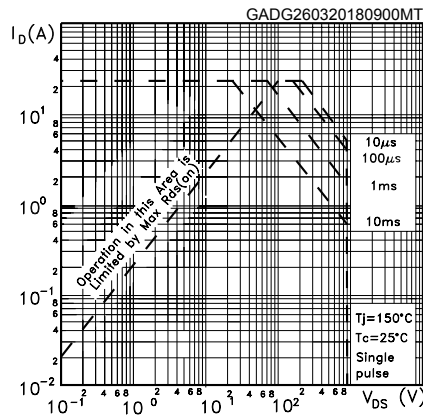
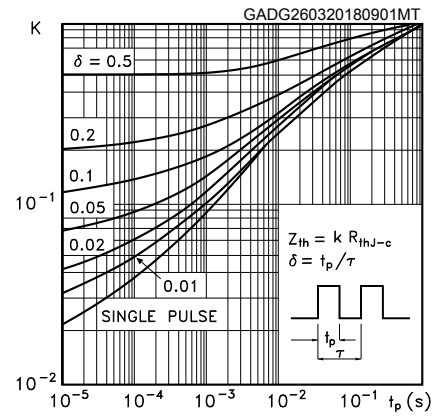
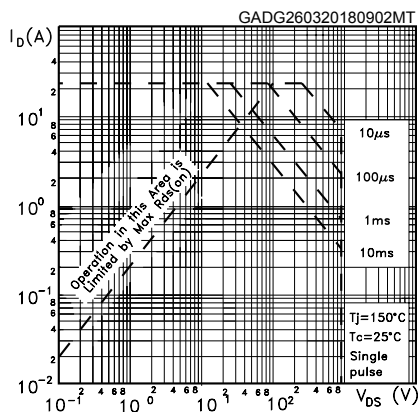
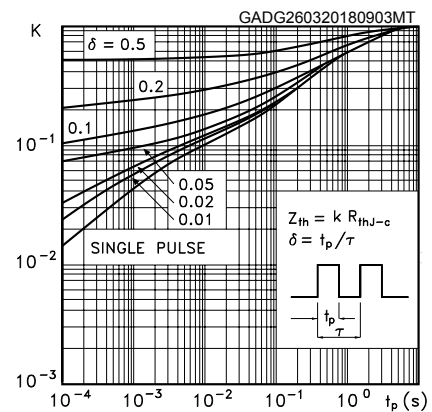
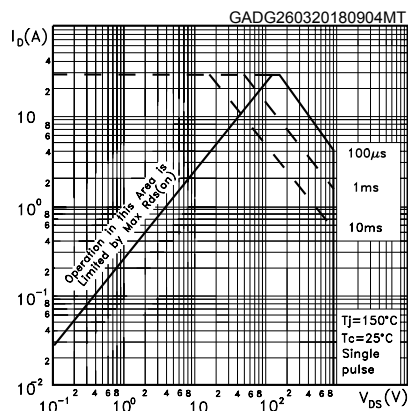
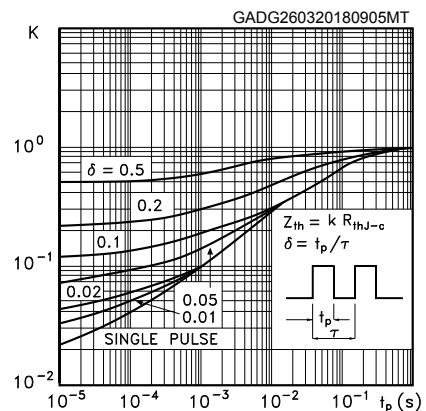
Figure 1. Safe operating area for TO-220/D²PAK

Figure 2. Thermal impedance for TO-220/D²PAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Safe operating area for TO-247

Figure 6. Thermal impedance for TO-247


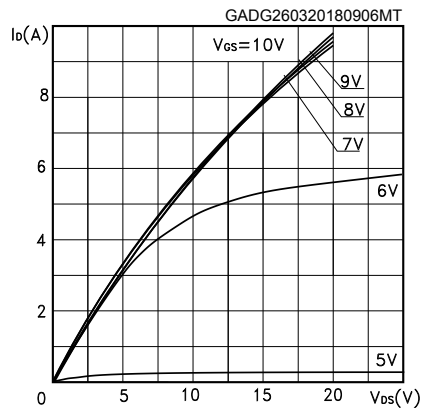
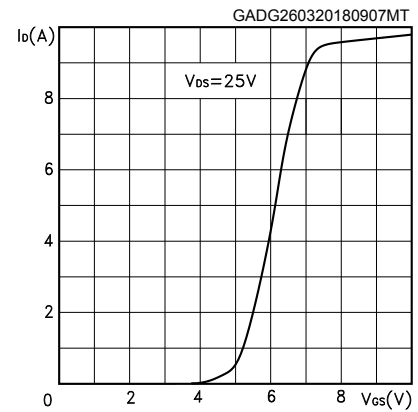
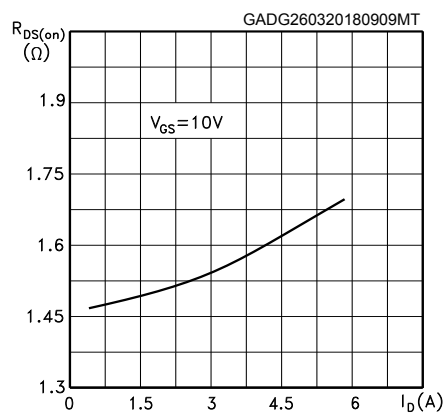
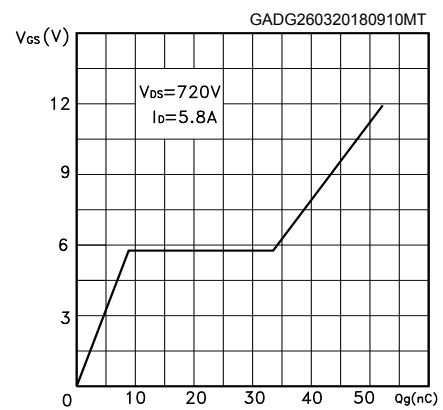
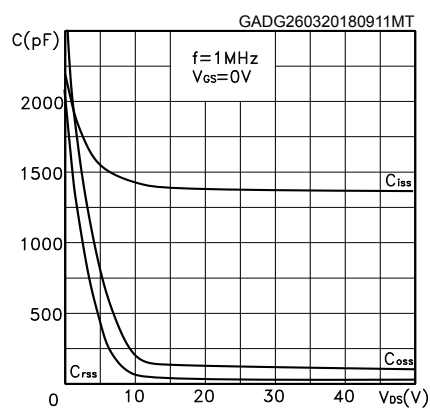
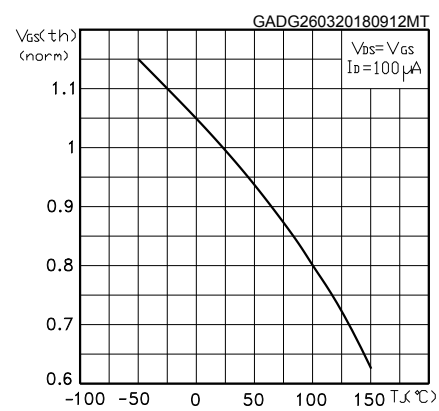
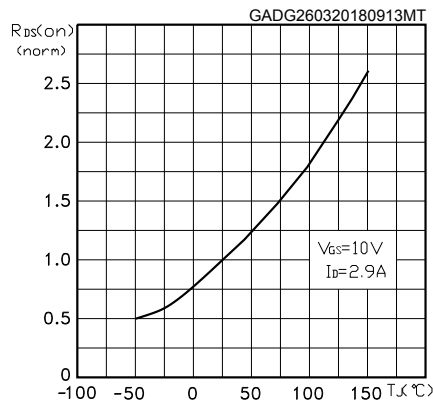
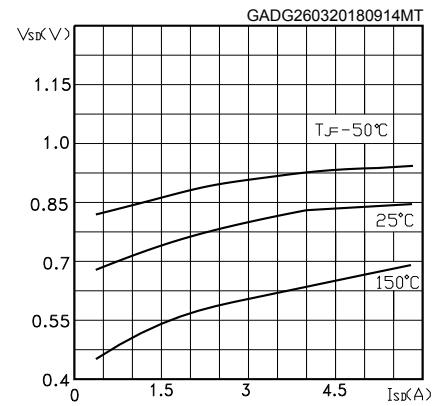
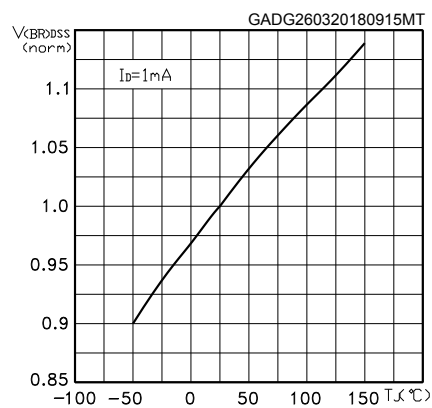
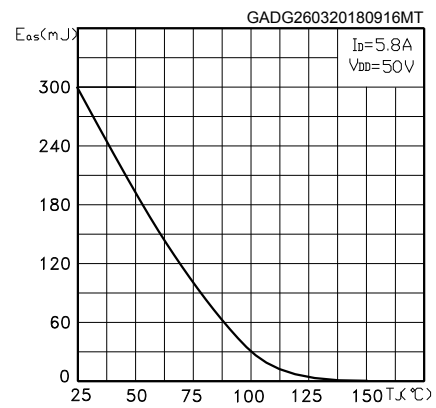
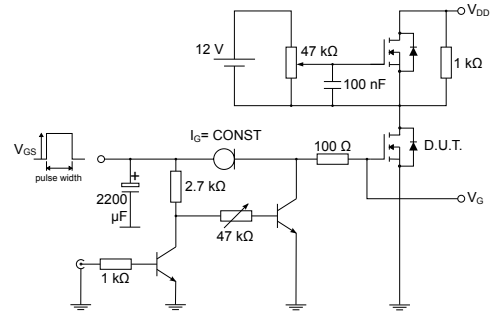
Figure 7. Output characteristics

Figure 8. Transfer characteristics

Figure 9. Static drain-source on resistance

Figure 10. Gate charge vs gate-source voltage

Figure 11. Capacitance variations

Figure 12. Normalized gate threshold voltage vs temperature


Figure 13. Normalized on resistance vs temperature

Figure 14. Source-drain diode forward characteristic

Figure 15. Normalized $V_{(BR)DSS}$ vs temperature

Figure 16. Maximum avalanche energy vs temperature


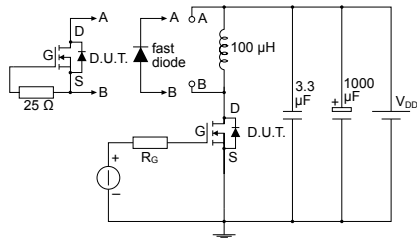
3 Test circuits

Figure 17. Test circuit for resistive load switching times

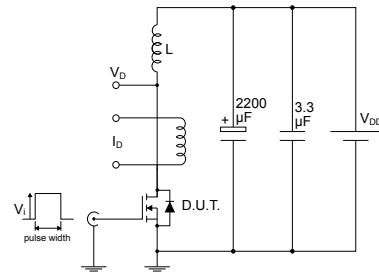

AM01468v1

Figure 18. Test circuit for gate charge behavior


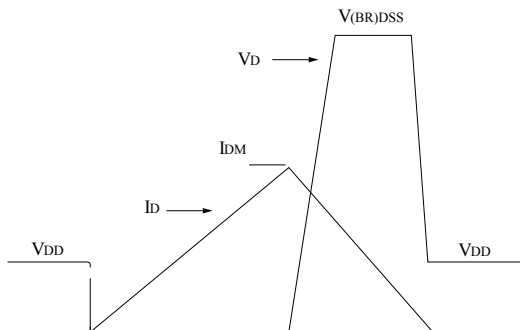
AM01469v1

Figure 19. Test circuit for inductive load switching and diode recovery times


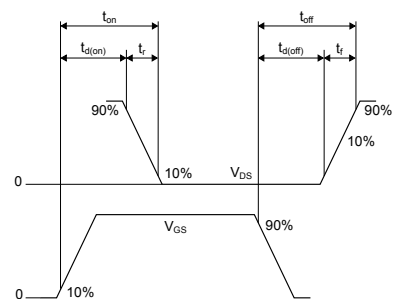
AM01470v1

Figure 20. Unclamped inductive load test circuit


AM01471v1

Figure 21. Unclamped inductive waveform


AM01472v1

Figure 22. Switching time waveform


AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) package information

Figure 23. D²PAK (TO-263) type A package outline



0079457_24

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Technical drawing of a rectangular component with dimensions and a cross-section. The drawing includes a top view, a front view, a side view, and a cross-section (c). Dimensions are labeled as follows:

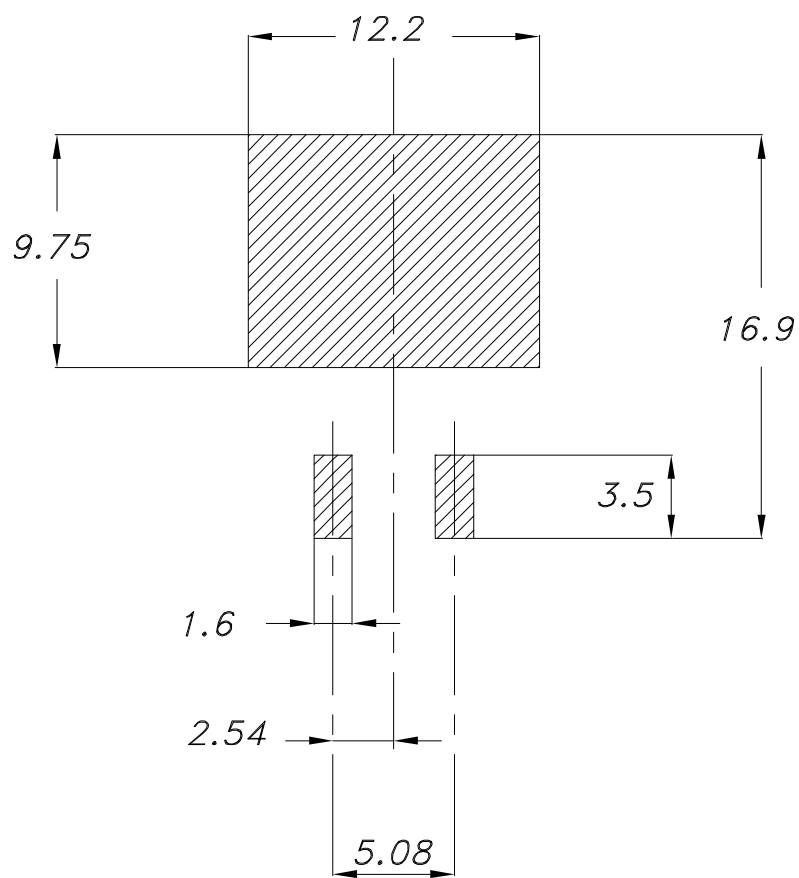
- Top View:** Dimensions E (width) and E_1 (inner width) are shown. A central slot is indicated.
- Front View:** Dimensions D (height), L_1 (top flange height), L_2 (bottom flange height), and H (total height) are shown. A central circular feature is indicated.
- Side View:** Dimensions A (width) and B (height) are shown. A central slot is indicated.
- Cross-section (c):** Dimensions c (width), c_2 (inner width), and c_1 (height) are shown. The cross-section is labeled **PLATING** and **BASE METAL**.
- Other Dimensions:** e (distance from center to side), $2x b_2$ (distance from center to side), $2x b$ (distance from center to side), b_1, b_3 (width), b, b_2 (width), L_3 (height), L_4 (height), A_1 (width), and H (height) are shown.
- Notes:** The drawing includes a note $0^\circ \sim 8^\circ$ indicating a taper angle.

page 12/26

Table 9. D²PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
b3	1.36		1.46
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

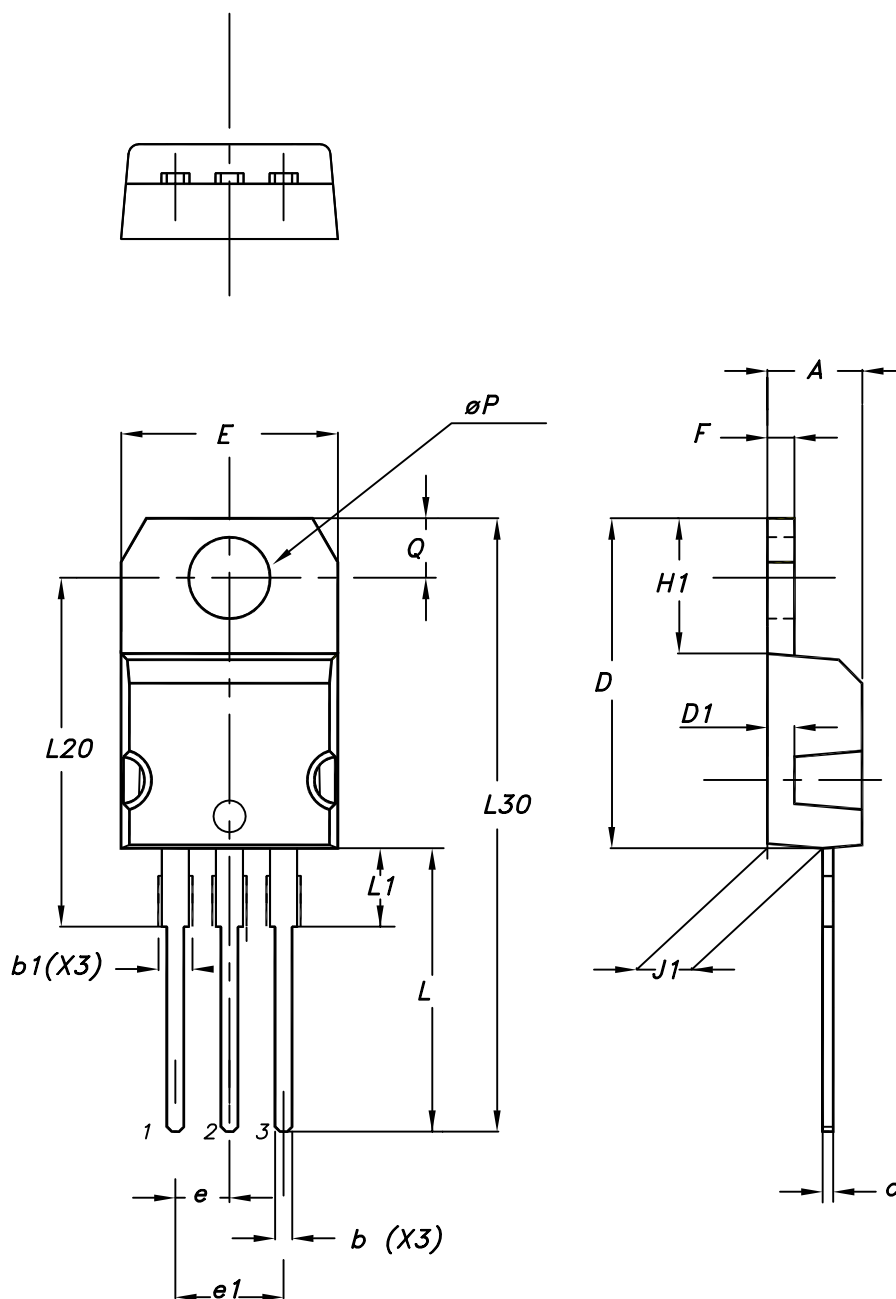
Figure 25. D²PAK (TO-263) recommended footprint (dimensions are in mm)



Footprint

4.2 TO-220 type A package information

Figure 26. TO-220 type A package outline



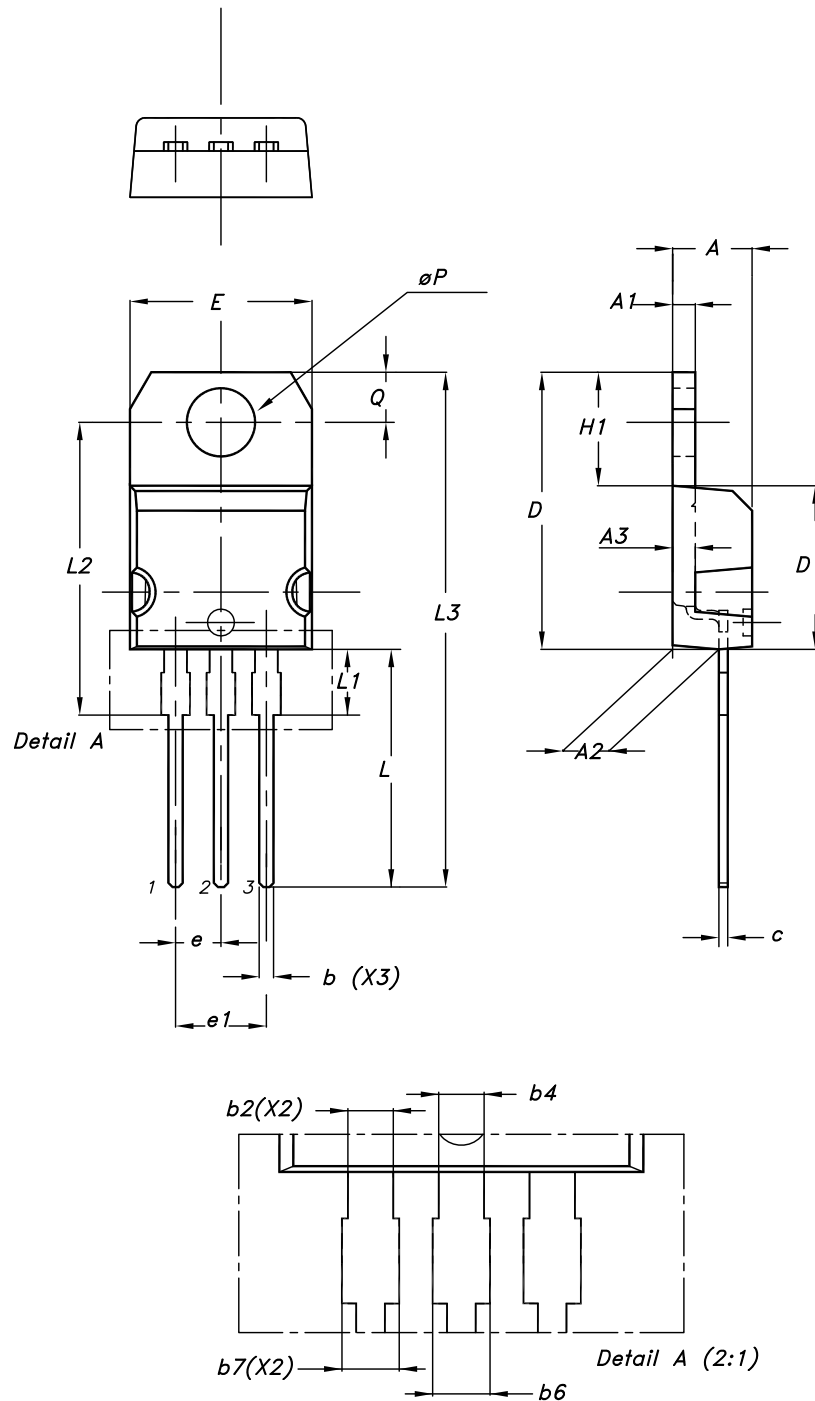
0015988_typeA_Rev_21

Table 10. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.3 TO-220 type H package information

Figure 27. TO-220 type H package outline



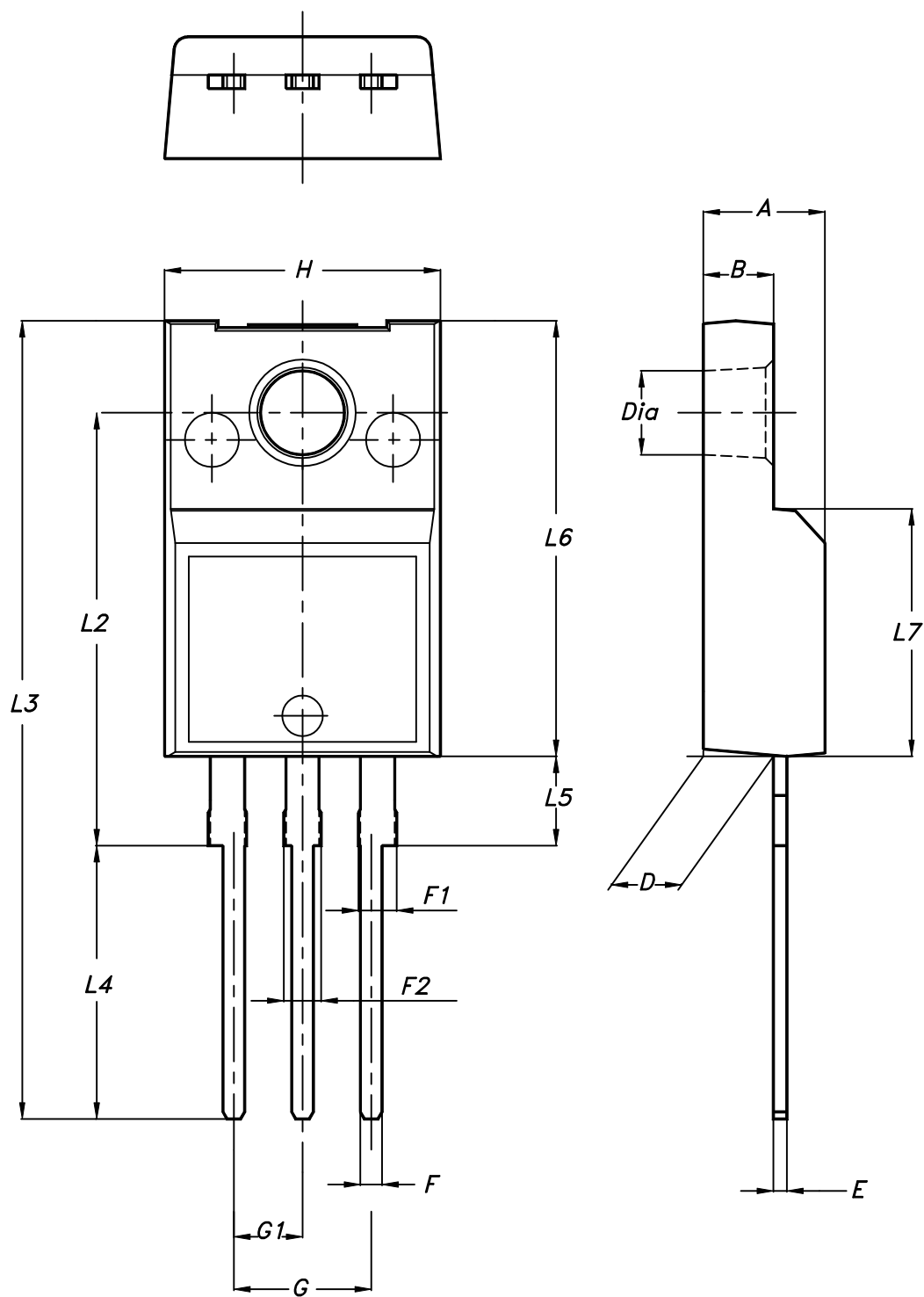
0015988_H_21

Table 11. TO-220 type H package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	4.45	4.50
A1	1.22		1.32
A2	2.49	2.59	2.69
A3	1.17	1.27	1.37
b	0.78		0.87
b2	1.25		1.34
b4	1.20		1.29
b6			1.50
b7			1.45
c	0.49		0.56
D	15.40	15.50	15.60
D1	9.05	9.15	9.25
E	10.08	10.18	10.28
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
H1	6.25	6.35	6.45
L	13.20	13.40	13.60
L1	3.50	3.70	3.90
L2	16.30	16.40	16.50
L3	28.70	28.90	29.10
ØP	3.75	3.80	3.85
Q	2.70	2.80	2.90

4.4 TO-220FP package information

Figure 28. TO-220FP package outline



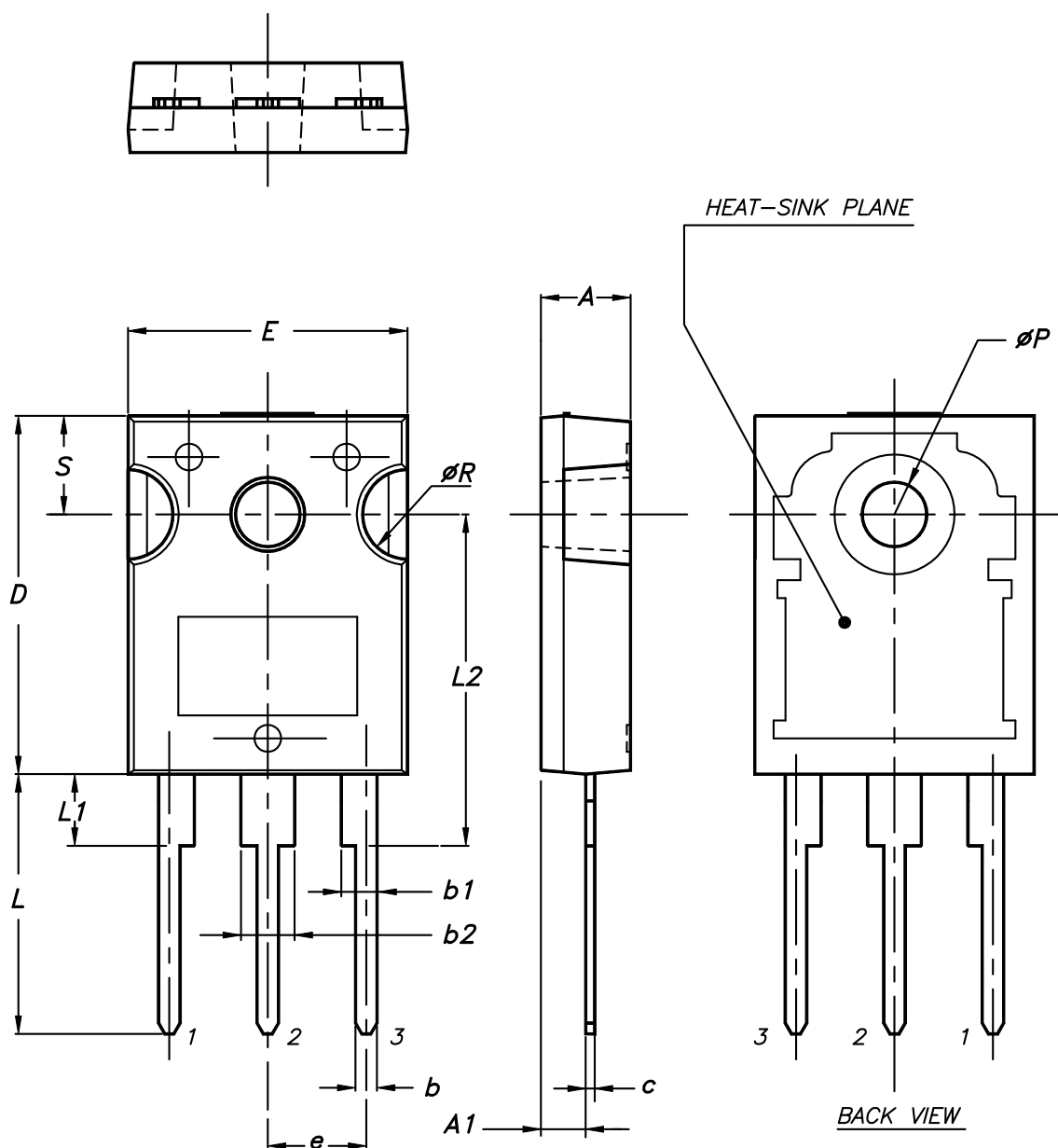
7012510_Rev_12_B

Table 12. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.5 TO-247 package information

Figure 29. TO-247 package outline



0075325_9

Table 13. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Ordering information

Table 14. Order codes

Order code	Marking	Package	Packing
STB6NK90ZT4	B6NK90Z	D ² PAK	Tape e reel
STP6NK90Z	P6NK90Z	TO-220	Tube
STP6NK90ZFP	P6NK90ZFP	TO-220FP	Tube
STW7NK90Z	W7NK90Z	TO-247	Tube

Revision history

Table 15. Document revision history

Date	Version	Changes
29-Nov-2005	3	Complete version
16-Aug-2006	4	New template, no content change
10-Apr-2007	5	Typo mistake on Table 2
04-Apr-2018	6	Removed maturity status indication from cover page. The document status is production data. Updated Table 5. Dynamic and Table 6. Source drain diode . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics curves	5
3	Test circuits	8
4	Package information.....	9
4.1	D ² PAK (TO-263) package information	9
4.2	TO-220 type A package information.....	14
4.3	TO-220 type H package information.....	16
4.4	TO-220FP package information	18
4.5	TO-247 package information.....	20
5	Ordering information	23
	Revision history	24



IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved