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Kind regards,

Team Nexperia



BSS84

P-channel enhancement mode vertical DMOS transistor

Rev. 06 — 16 December 2008

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode vertical Diffusion Metal-Oxide Semiconductor (DMOS) transistor in a small Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number ^[1]	Package	
	NXP	JEDEC
BSS84	SOT23	TO-236AB
BSS84/DG		

[1] /DG: halogen-free

1.2 Features

- Low threshold voltage
- High-speed switching
- Direct interface to CMOS and Transistor-Transistor Logic (TTL)
- No secondary breakdown

1.3 Applications

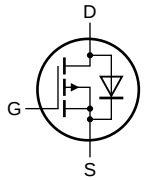
- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers

1.4 Quick reference data

- $V_{DS} \leq -50 \text{ V}$
- $I_D \leq -130 \text{ mA}$
- $R_{DS(on)} \leq 10 \text{ } \Omega$
- $P_{tot} \leq 250 \text{ mW}$

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT23 (TO-236AB)	 001aaa025
2	S	source		
3	D	drain		

3. Ordering information

Table 3. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
BSS84	TO-236AB	plastic surface-mounted package; 3 leads	SOT23
BSS84/DG			

[1] /DG: halogen-free

4. Marking

Table 4. Marking codes

Type number ^[1]	Marking code ^[2]
BSS84	13*
BSS84/DG	ZV*

[1] /DG: halogen-free

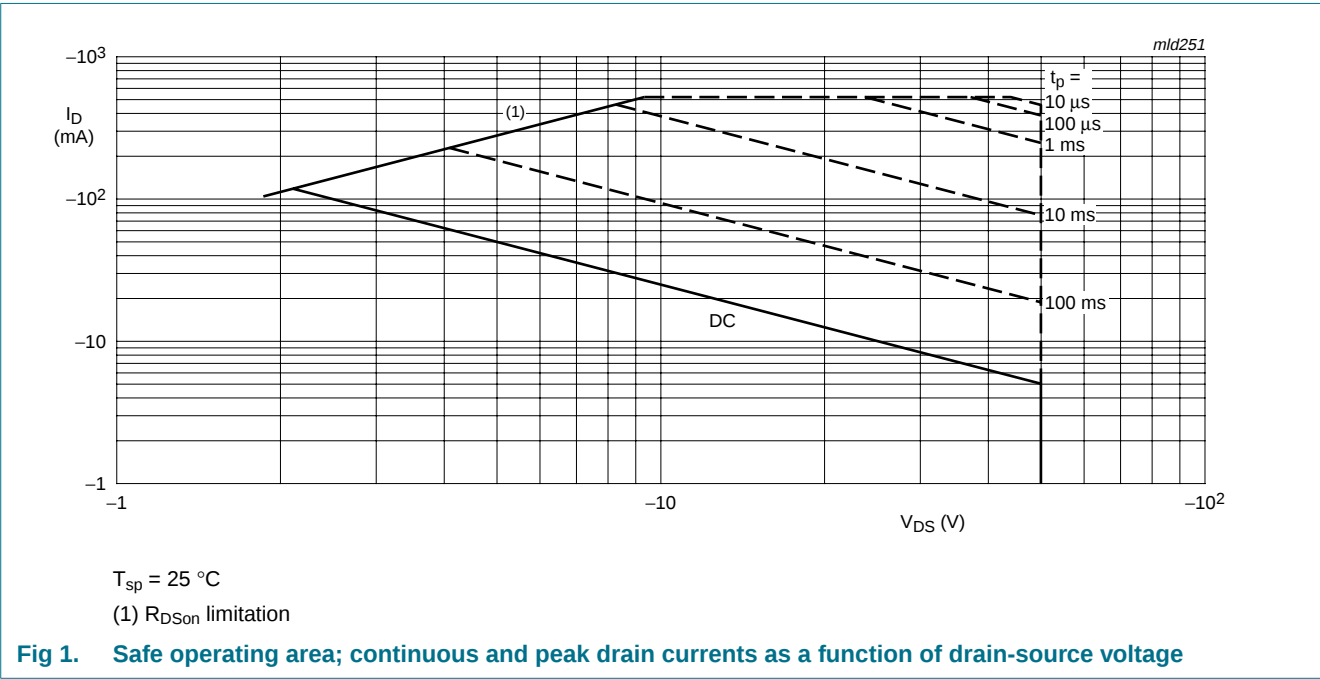
[2] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$	-	-50	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}; V_{GS} = -10\text{ V};$ see Figure 1	-	-130	mA
		$T_{sp} = 100\text{ }^{\circ}\text{C};$ $V_{GS} = -10\text{ V}$	-	-75	mA
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}; t_p \leq 10\text{ }\mu\text{s};$ see Figure 1	-	-520	mA
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C};$ see Figure 2 [1]	-	250	mW
T_{stg}	storage temperature		-65	+150	$^{\circ}\text{C}$
T_j	junction temperature		-65	+150	$^{\circ}\text{C}$

[1] Device mounted on a Printed-Circuit Board (PCB).



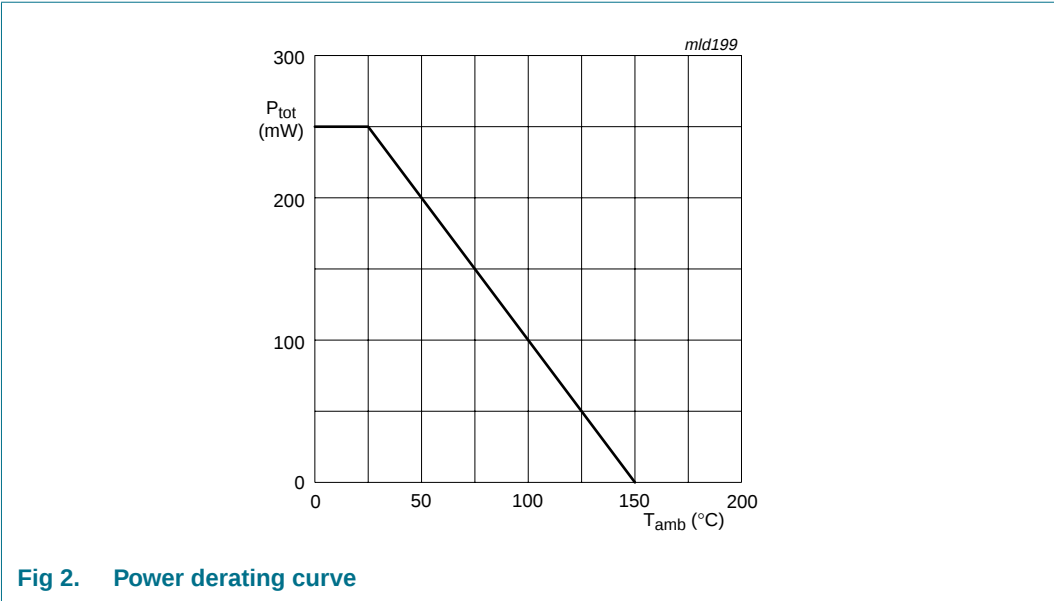


Fig 2. Power derating curve

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	see Figure 3	[1]	-	500	K/W

[1] Mounted on a PCB, vertical in still air.

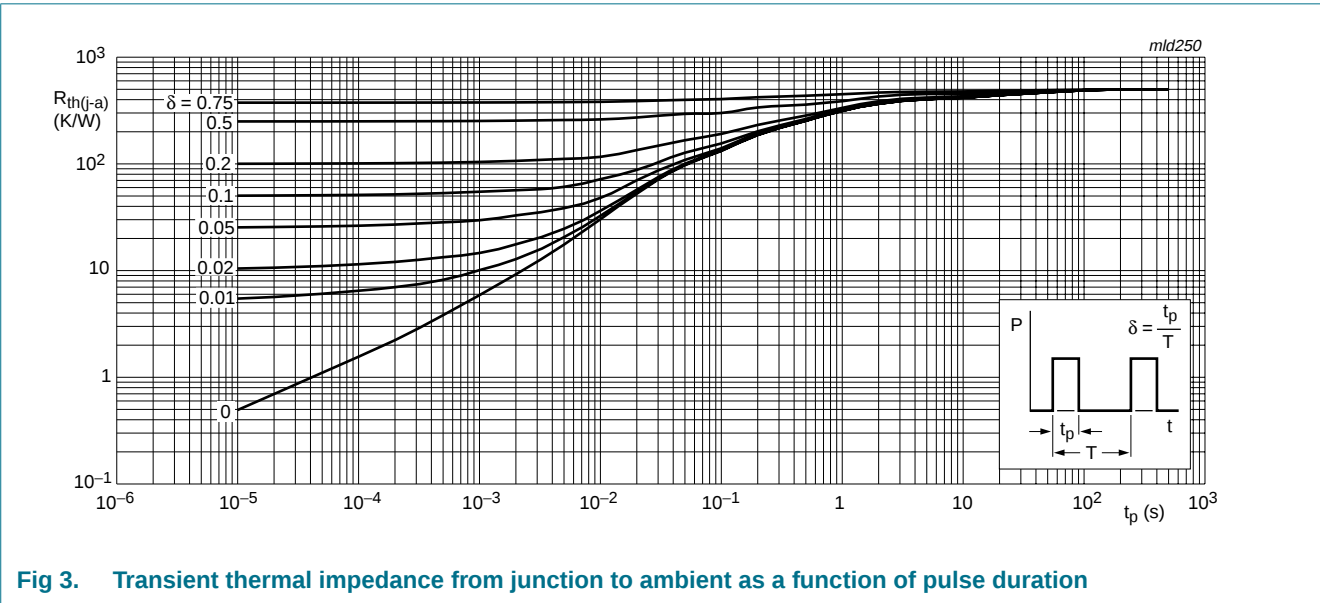


Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration

7. Characteristics

Table 7. Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -10\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$	-50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -1\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-0.8	-	-2	V
		$T_j = -55\text{ }^{\circ}\text{C}$	-	-	-1.8	V
I_{DSS}	drain leakage current	$V_{DS} = -40\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	-100	nA
		$V_{DS} = -50\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	-10	μA
I_{GSS}	gate leakage current	$T_j = 125\text{ }^{\circ}\text{C}$	-	-	-60	μA
		$V_{GS} = +20\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	100	nA
		$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}$; $I_D = -130\text{ mA}$; see Figure 5 and 7	-	6	10	Ω
Dynamic characteristics						
$ Y_{fs} $	transfer admittance	$V_{DS} = -25\text{ V}$; $I_D = -130\text{ mA}$	50	-	-	mS
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = -25\text{ V}$; $f = 1\text{ MHz}$; see Figure 9	-	25	45	pF
C_{oss}	output capacitance		-	15	25	pF
C_{rss}	reverse transfer capacitance		-	3.5	12	pF
t_{on}	turn-on time	$V_{DS} = -40\text{ V}$; $V_{GS} = 0\text{ V}$ to -10 V ; $I_D = -200\text{ mA}$; see Figure 10 and 11	-	3	-	ns
t_{off}	turn-off time	$V_{DS} = -40\text{ V}$; $V_{GS} = -10\text{ V}$ to 0 V ; $I_D = -200\text{ mA}$; see Figure 10 and 11	-	7	-	ns

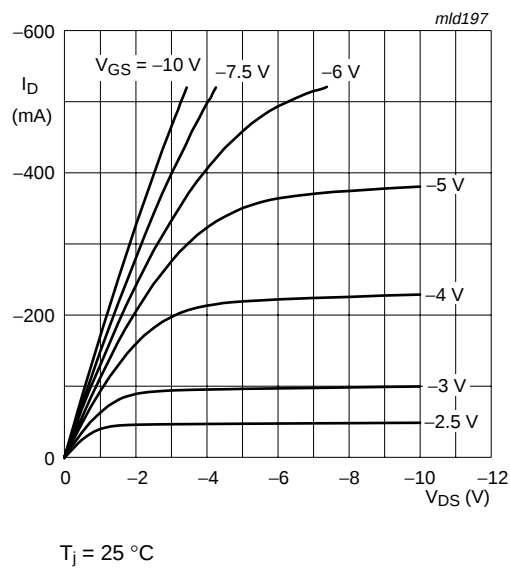


Fig 4. Output characteristics: drain current as a function of drain-source voltage; typical values

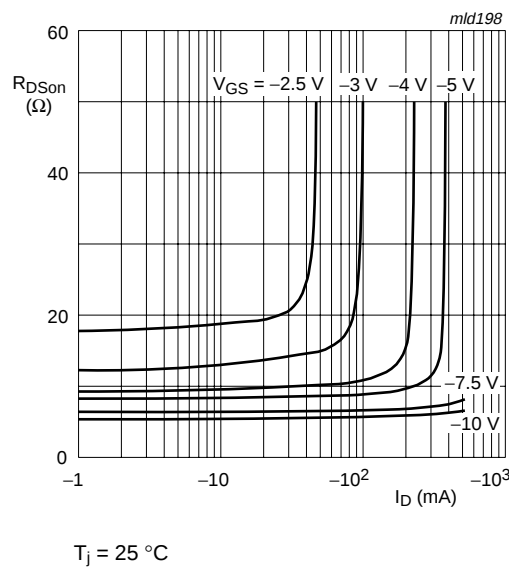


Fig 5. Drain-source on-state resistance as a function of drain current; typical values

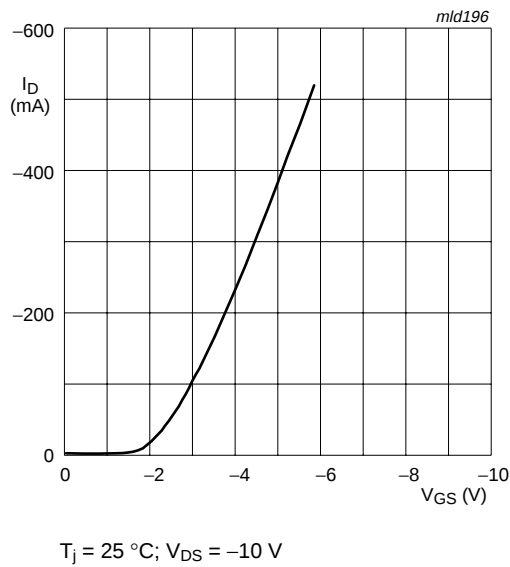


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

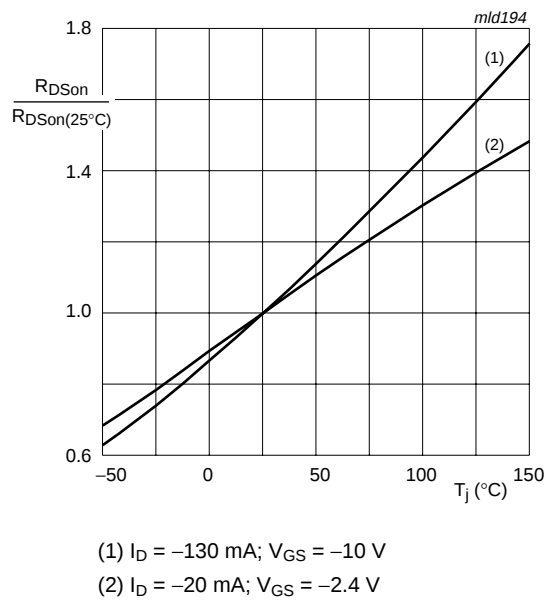
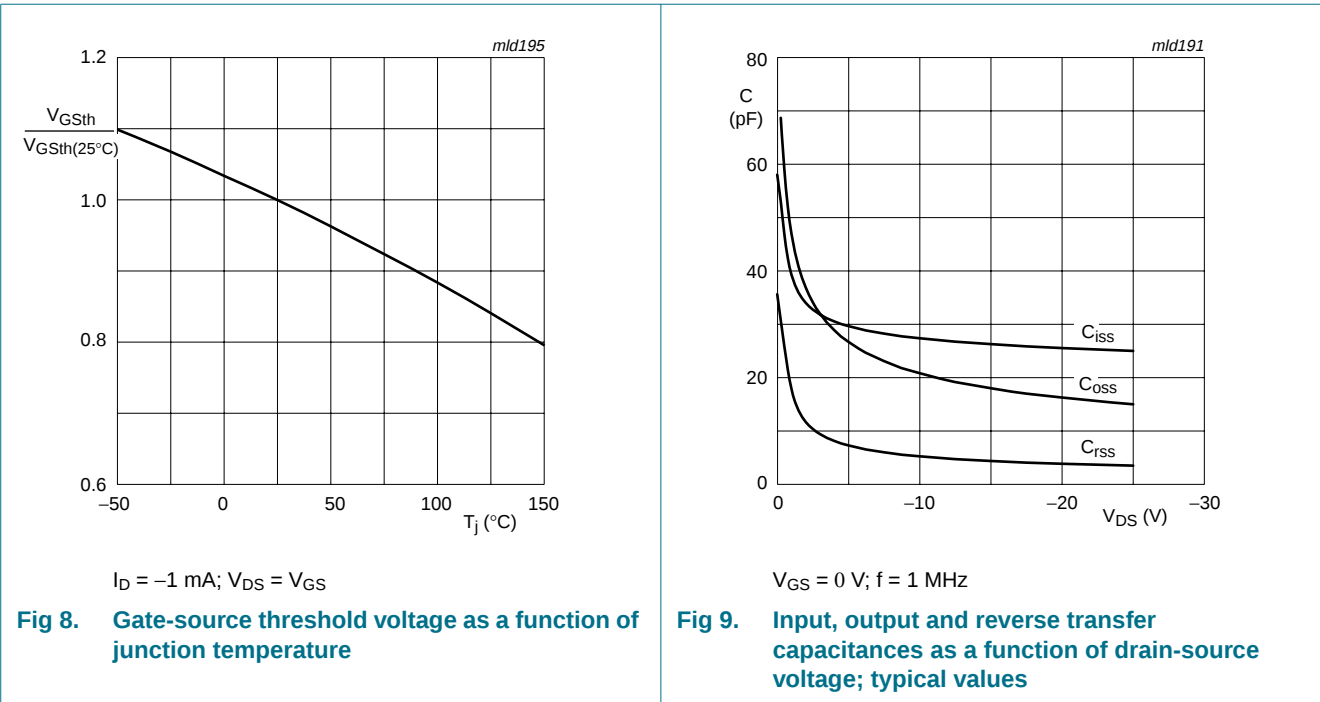
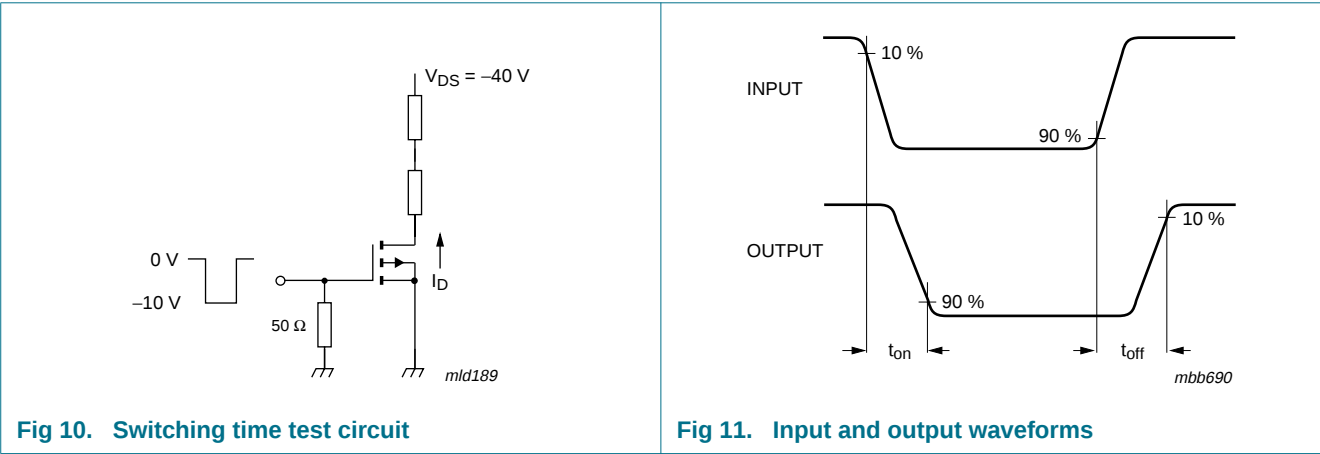


Fig 7. Normalized drain-source on-state resistance factor as a function of junction temperature



8. Test information



9. Package outline

Plastic surface-mounted package; 3 leads

SOT23

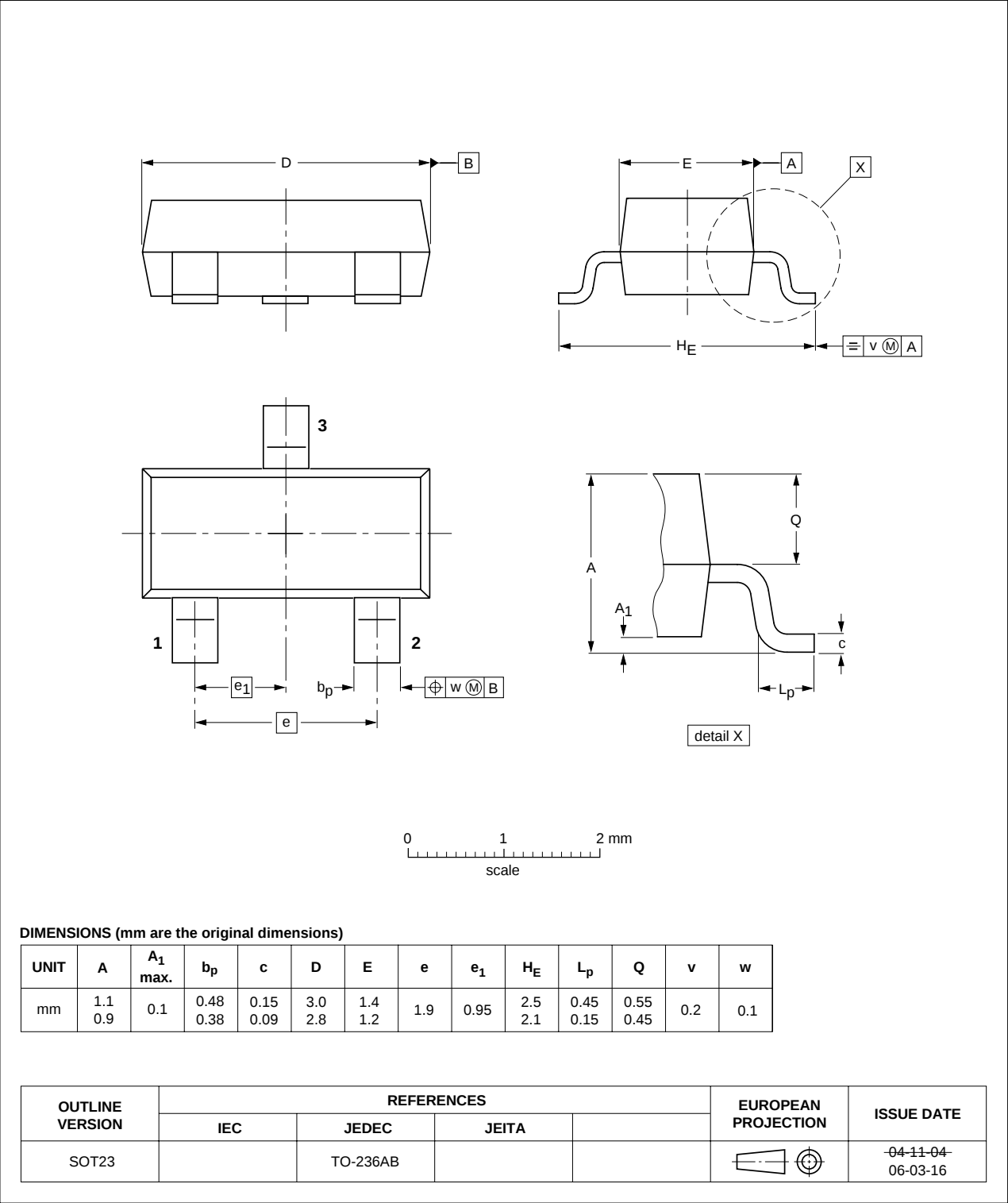


Fig 12. Package outline SOT23 (TO-236AB)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS84_6	20081216	Product data sheet	-	BSS84_5
Modifications:	• Table 5 “Limiting values” : P_{tot} figure reference updated			
BSS84_5	20081209	Product data sheet	-	BSS84_4
BSS84_4	20070717	Product data sheet	-	BSS84_3
BSS84_3	20030804	Product specification	-	BSS84_2
BSS84_2	19970618	Product specification	-	BSS84_1
BSS84_1	19950407	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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