



FDMS9620S

Dual N-Channel PowerTrench[®] MOSFET

Q1: 30V, 16A, 21.5mΩ Q2: 30V, 18A, 13mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 21.5mΩ at V_{GS} = 10V, I_D = 7.5A
- Max $r_{DS(on)}$ = 29.5mΩ at V_{GS} = 4.5V, I_D = 6.5A

Q2: N-Channel

- Max $r_{DS(on)}$ = 13mΩ at V_{GS} = 10V, I_D = 10A
- Max $r_{DS(on)}$ = 17mΩ at V_{GS} = 4.5V, I_D = 8.5A
- Low Qg high side MOSFET
- Low $r_{DS(on)}$ low side MOSFET
- Thermally efficient dual Power 56 package
- Pinout optimized for simple PCB design
- RoHS Compliant



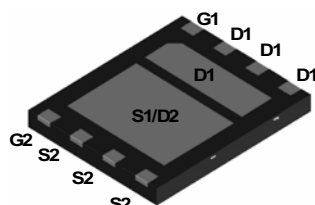
General Description

This device includes two specialized MOSFETs in a unique dual Power 56 package. It is designed to provide an optimal Synchronous Buck power stage in terms of efficiency and PCB utilization. The low switching loss "High Side" MOSFET is complemented by a Low Conduction Loss "Low Side" SyncFET.

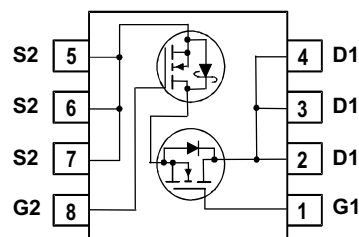
Applications

Synchronous Buck Converter for:

- Notebook System Power
- General Purpose Point of Load



Power 56



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V _{DS}	Drain to Source Voltage	30	30	V
V _{GS}	Gate to Source Voltage	±20	±20	V
I _D	Drain Current -Continuous			

Thermal Characteristics

R _{θJC}	Thermal Resistance, Junction to Case	8.2	3.1	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	50		
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1b)	120		

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS9620S	FDMS9620S	Power 56	13"	12mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ $I_D = 1\text{mA}$, $V_{GS} = 0\text{V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = 1\text{mA}$, referenced to 25°C	Q1 Q2		23 23		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$	Q1 Q2			1 500	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$	Q1 Q2			± 100 ± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = 1\text{mA}$	Q1 Q2	1 1	1.6 1.6	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = 1\text{mA}$, referenced to 25°C	Q1 Q2		-4 -4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 7.5\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 6.5\text{A}$ $V_{GS} = 10\text{V}$, $I_D = 7.5\text{A}$, $T_J = 125^\circ\text{C}$	Q1		18 23 25	21.5 29.5 32	m Ω
		$V_{GS} = 10\text{V}$, $I_D = 10\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 8.5\text{A}$ $V_{GS} = 10\text{V}$, $I_D = 10\text{A}$, $T_J = 125^\circ\text{C}$	Q2		9 13 14	13 17 22	
g_{FS}	Forward Transconductance	$V_{DD} = 10\text{V}$, $I_D = 7.5\text{A}$ $V_{DD} = 10\text{V}$, $I_D = 10\text{A}$	Q1 Q2		25 27		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	Q1 Q2		500 700	665 935	pF
C_{oss}	Output Capacitance		Q1 Q2		100 500	135 665	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		65 100	100 150	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	Q1 Q2		0.9 1.8		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}$, $I_D = 1\text{A}$, $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$	Q1 Q2		11 15	20 27	ns
t_r	Rise Time		Q1 Q2		7 13	14 24	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		23 27	37 44	ns
t_f	Fall Time		Q1 Q2		2.3 7	10 14	ns
Q_g	Total Gate Charge	Q1 $V_{DD} = 15\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 7.5\text{A}$	Q1 Q2		10 18	14 25	nC
Q_{gs}	Gate to Source Gate Charge	Q2 $V_{DD} = 15\text{V}$, $V_{GS} = 10\text{V}$, $I_D = 10\text{A}$	Q1 Q2		1.7 2.8		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		2.0 3.6		nC

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			2.1 3.5	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}$, $I_S = 2.1\text{A}$ (Note 2) $V_{GS} = 0\text{V}$, $I_S = 3.5\text{A}$ (Note 2)	Q1 Q2		0.7 0.5	1.2 1.0	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 7.5\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$	Q1 Q2		13 14		ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = 10\text{A}$, $di/dt = 300\text{A}/\mu\text{s}$	Q1 Q2		4 9		nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on
a 1in^2 pad of 2 oz copper



b. $120^\circ\text{C}/\text{W}$ when mounted on a
minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < $300\mu\text{s}$, Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

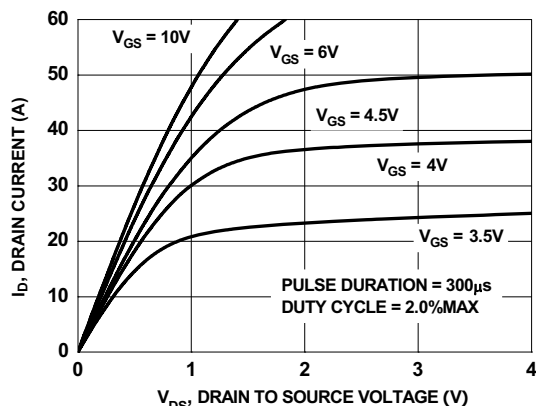


Figure 1. On Region Characteristics

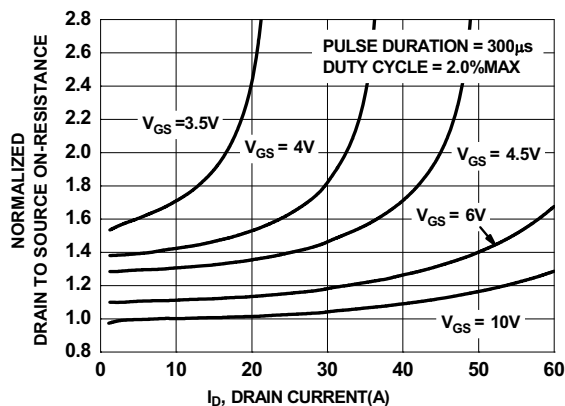


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

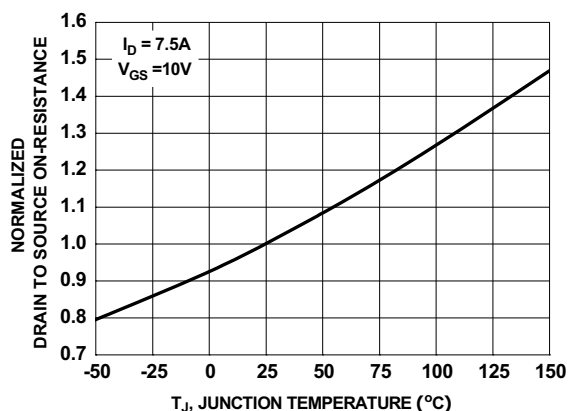


Figure 3. Normalized On Resistance vs Junction Temperature

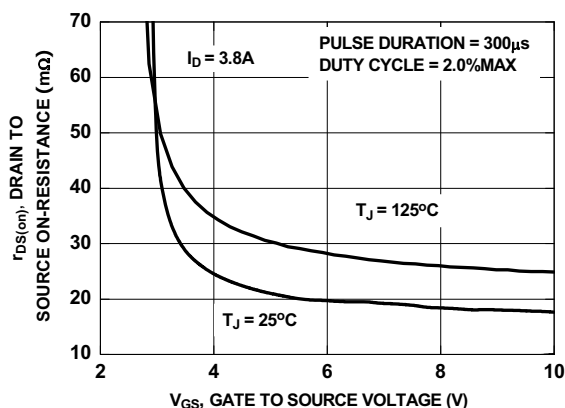


Figure 4. On-Resistance vs Gate to Source Voltage

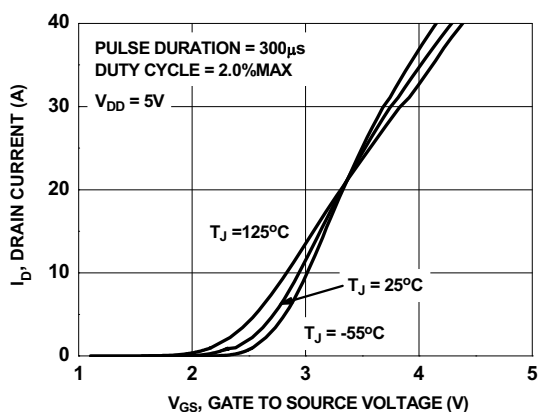


Figure 5. Transfer Characteristics

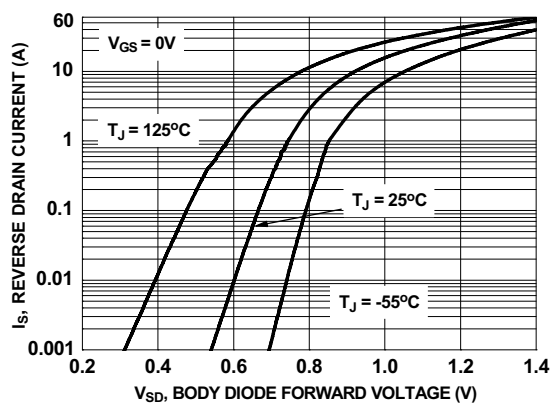


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

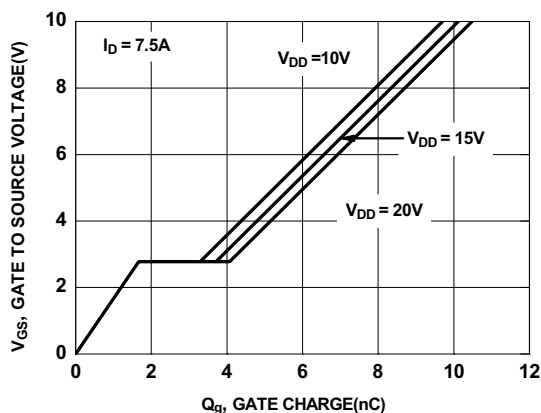


Figure 7. Gate Charge Characteristics

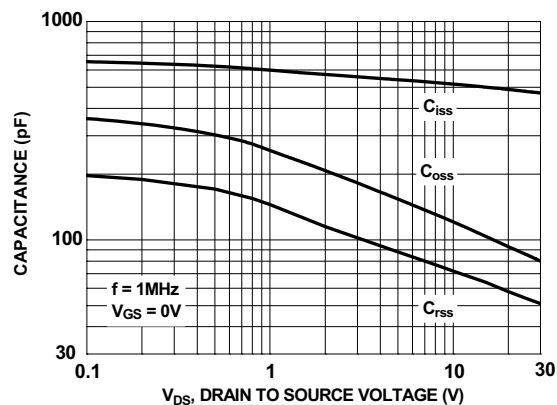


Figure 8. Capacitance vs Drain to Source Voltage

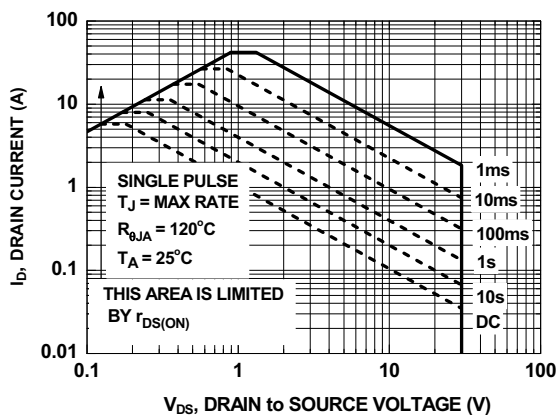


Figure 9. Forward Bias Safe Operating Area

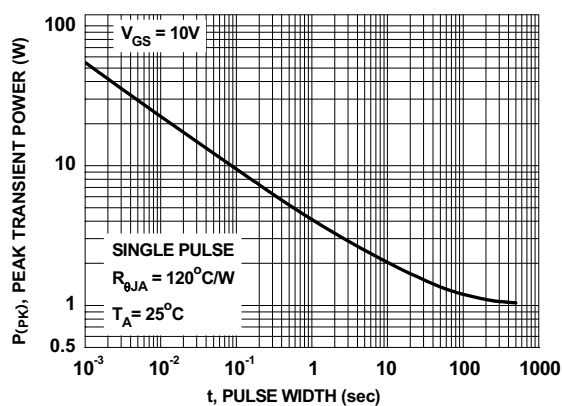


Figure 10. Single Pulse Maximum Power Dissipation

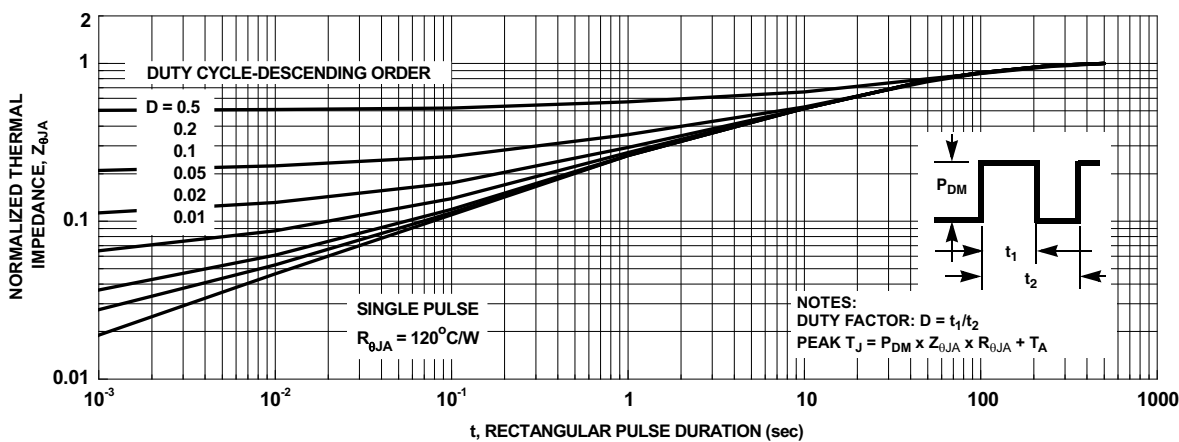


Figure 11. Transient Thermal Response Curve

Typical Characteristics (Q2 SyncFET)

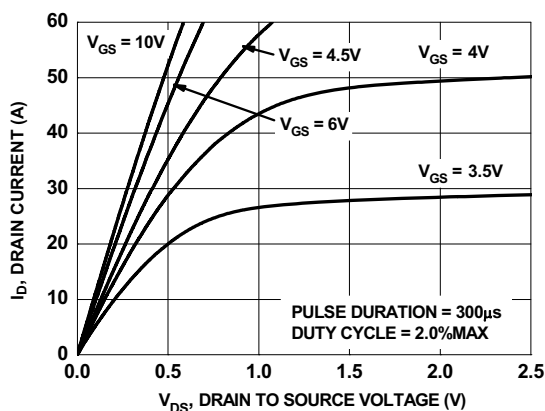


Figure 12. On-Region Characteristics

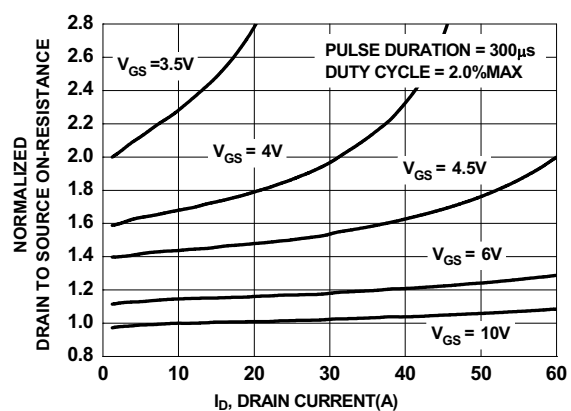


Figure 13. Normalized on-Resistance vs Drain Current and Gate Voltage

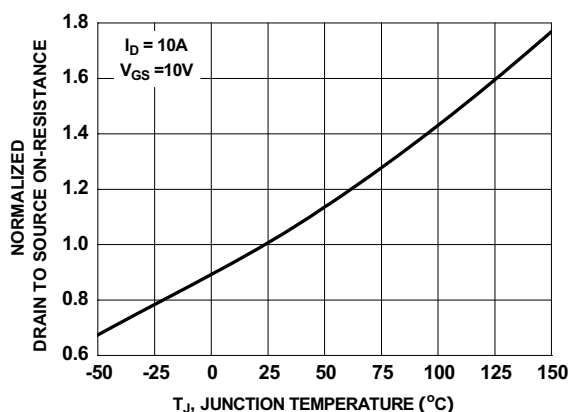


Figure 14. Normalized On-Resistance vs Junction Temperature

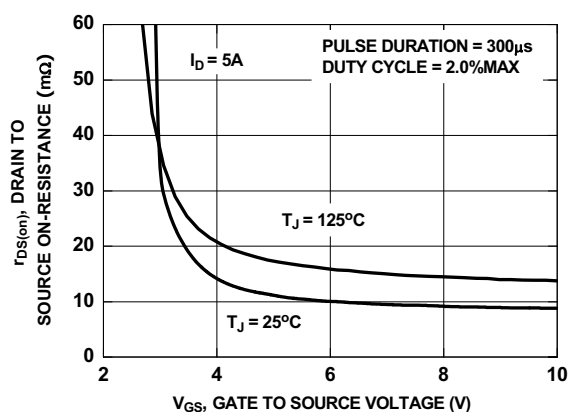


Figure 15. On-Resistance vs Gate to Source Voltage

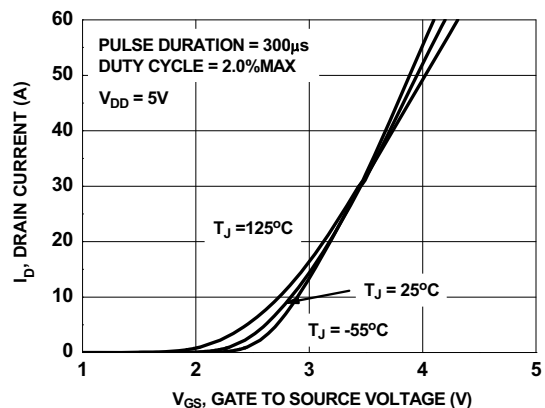


Figure 16. Transfer Characteristics

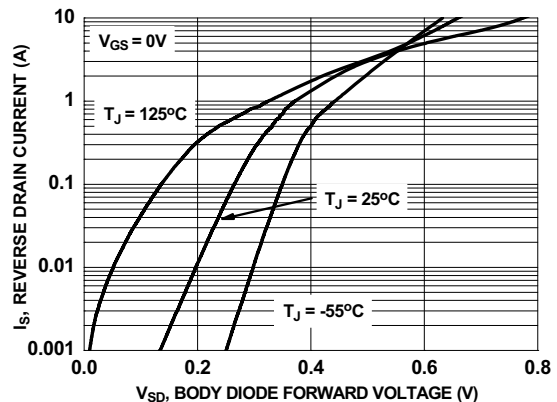


Figure 17. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

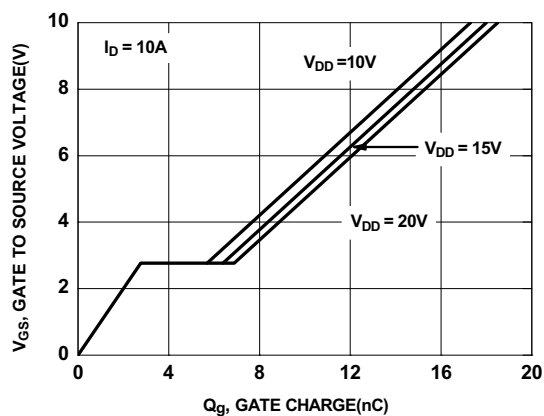


Figure 18. Gate Charge Characteristics

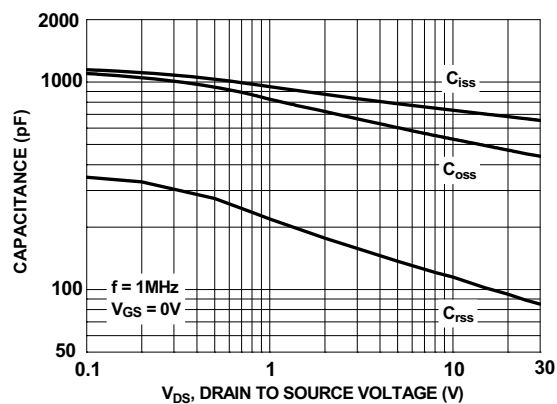
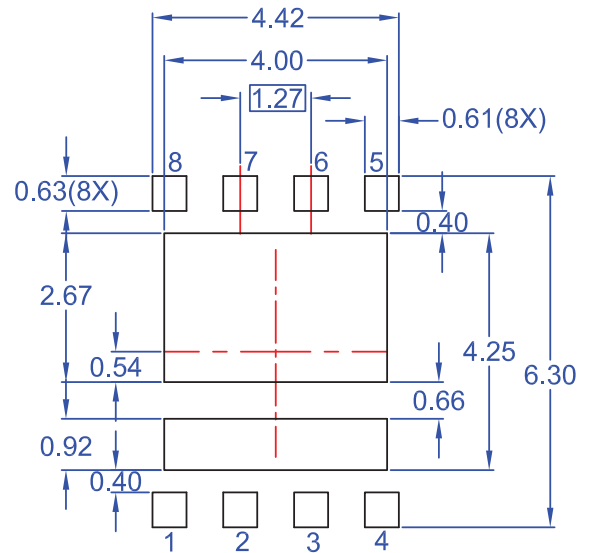
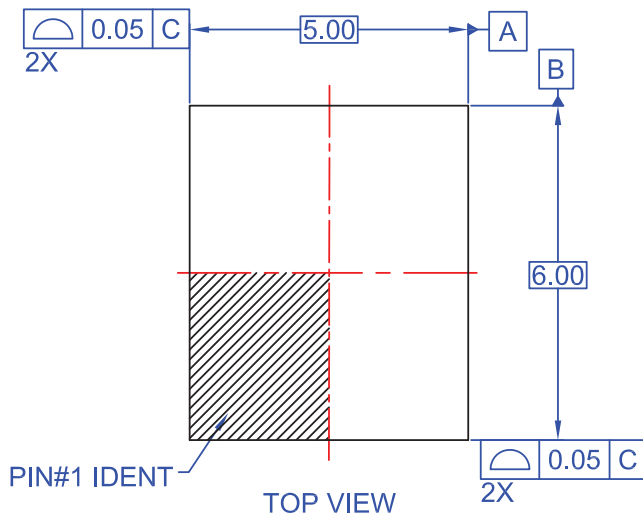
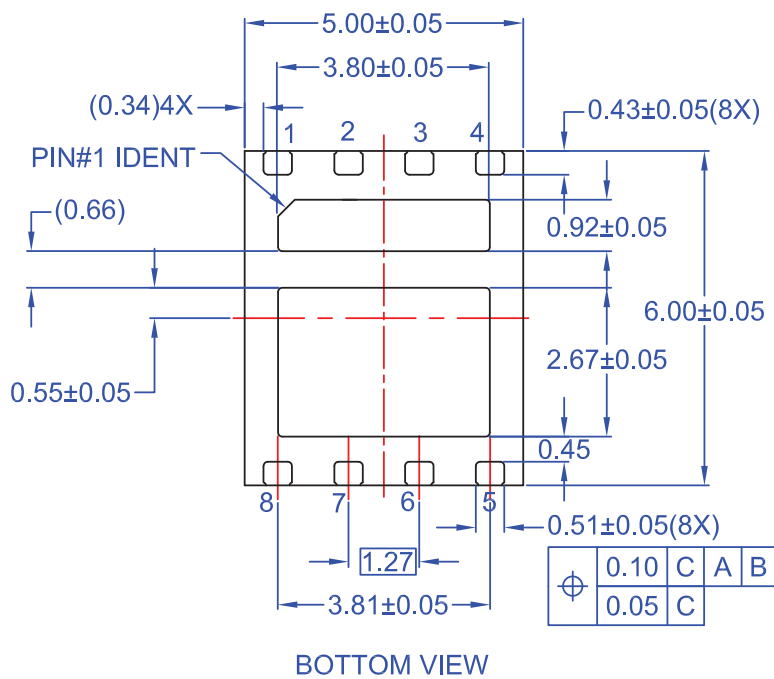
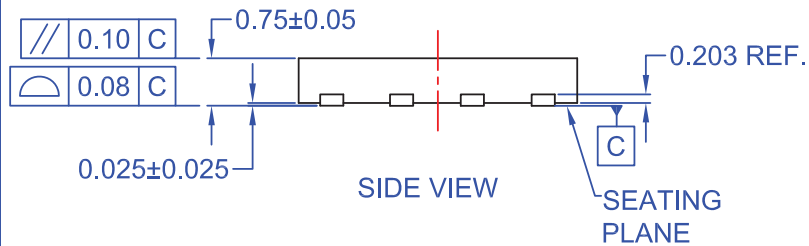


Figure 19. Capacitance vs Drain to Source Voltage



NOTE:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Krev3.



⌀	0.10	C	A	B
	0.05	C		



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AttitudeEngine™
Awinda®
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource™
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
MotionGrid®
MTI®
MTX®
MVN®
mWSaver®
OptoHit™
OPTOLOGIC®

OPTOPLANAR®
Power Supply WebDesigner™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™

SYSTEM GENERAL®*
TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
μSerDes™
SerDes®
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™
Xsens™
仙童®

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. TO OBTAIN THE LATEST, MOST UP-TO-DATE DATASHEET AND PRODUCT INFORMATION, VISIT OUR WEBSITE AT [HTTP://WWW.FAIRCHILDSEMI.COM](http://www.fairchildsemi.com). FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

AUTHORIZED USE

Unless otherwise specified in this data sheet, this product is a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability. This product may not be used in the following applications, unless specifically approved in writing by a Fairchild officer: (1) automotive or other transportation, (2) military/aerospace, (3) any safety critical application – including life critical medical equipment – where the failure of the Fairchild product reasonably would be expected to result in personal injury, death or property damage. Customer's use of this product is subject to agreement of this Authorized Use policy. In the event of an unauthorized use of Fairchild's product, Fairchild accepts no liability in the event of product failure. In other respects, this product shall be subject to Fairchild's Worldwide Terms and Conditions of Sale, unless a separate agreement has been signed by both Parties.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Terms of Use

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I77