

N-Channel 200 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
200	0.090 at $V_{GS} = 10$ V	19
	0.105 at $V_{GS} = 6$ V	17.5

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

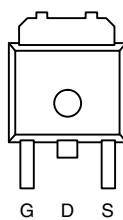


RoHS
COMPLIANT

APPLICATIONS

- Primary Side Switch

TO-252

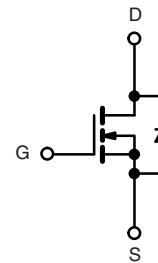


Top View

Drain Connected to Tab

Ordering Information:

SUD19N20-90-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175\text{ }^{\circ}\text{C}$) ^b	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	19	A
	$T_C = 125\text{ }^{\circ}\text{C}$		11	
Pulsed Drain Current		I_{DM}	40	
Continuous Source Current (Diode Conduction)		I_S	19	
Avalanche Current		I_{AS}	19	
Single Pulse Avalanche Energy	L = 0.1 mH	E_{AS}	18	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	136 ^b	W
	$T_A = 25\text{ }^{\circ}\text{C}$		3 ^a	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ s	15	°C/W
		Steady State	40	
Junction-to-Case (Drain)	R_{thJC}	0.85	1.1	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See SOA curve for voltage derating.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	200			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V			1	μA
		V _{DS} = 200 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 200 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	40			A
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 5 A		0.075	0.090	Ω
		V _{GS} = 10 V, I _D = 5 A, T _J = 125 °C			0.190	
		V _{GS} = 10 V, I _D = 5 A, T _J = 175 °C			0.260	
		V _{GS} = 6 V, I _D = 5 A		0.082	0.105	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 19 A		35		S
Dynamic ^a						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, F = 1 MHz		1800		pF
Output Capacitance	C _{oss}			180		
Reverse Transfer Capacitance	C _{rss}			80		
Total Gate Charge ^c	Q _g	V _{DS} = 100 V, V _{GS} = 10 V, I _D = 19 A		34	51	nC
Gate-Source Charge ^c	Q _{gs}			8		
Gate-Drain Charge ^c	Q _{gd}			12		
Gate Resistance	R _g		0.5		2.9	Ω
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 100 V, R _L = 5.2 Ω I _D ≡ 19 A, V _{GEN} = 10 V, R _g = 2.5 Ω		15	25	ns
Rise Time ^c	t _r			50	75	
Turn-Off Delay Time ^c	t _{d(off)}			30	45	
Fall Time ^c	t _f			60	90	
Source-Drain Diode Ratings and Characteristics (T _C = 25 °C)						
Pulsed Current	I _{SM}				50	A
Diode Forward Voltage ^b	V _{SD}	I _F = 19 A, V _{GS} = 0 V		0.9	1.5	V
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 19 A, dI/dt = 100 A/μs		180	250	ns

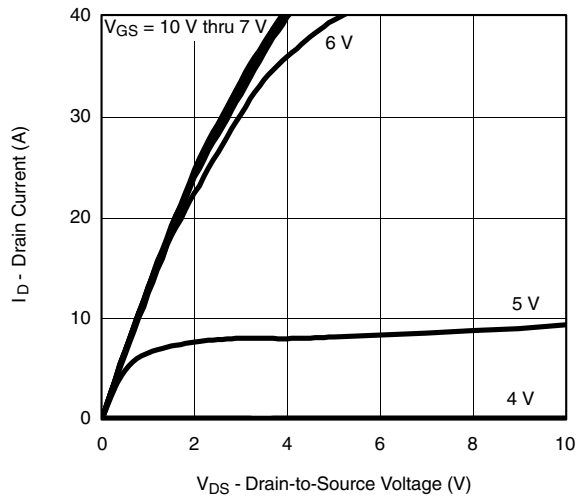
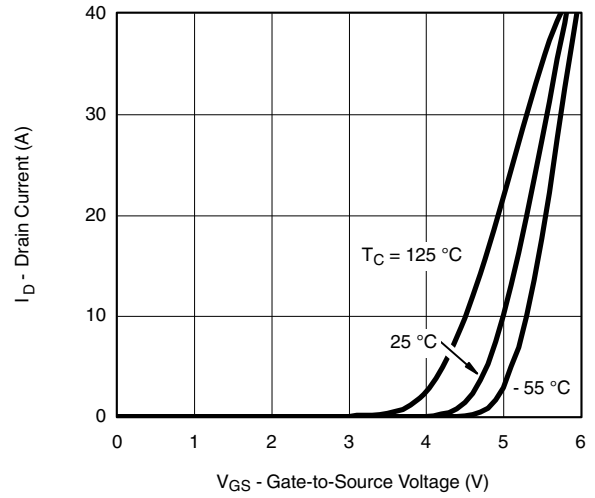
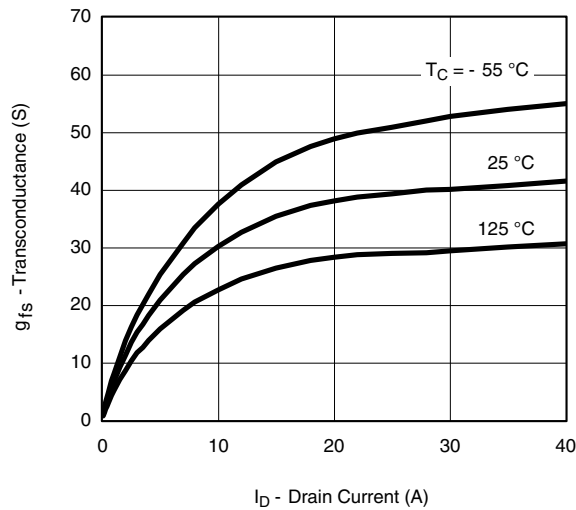
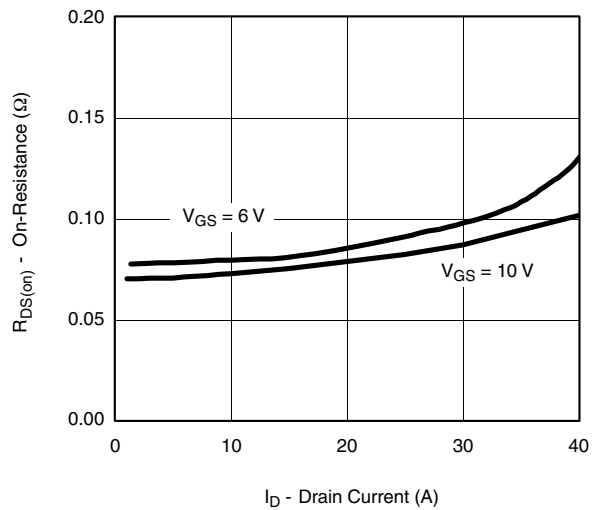
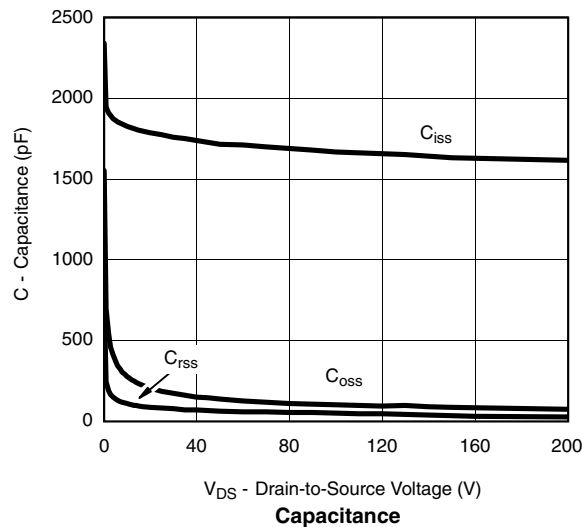
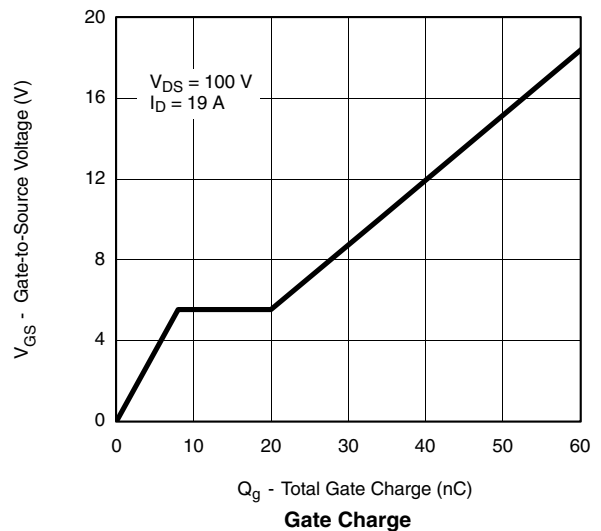
Notes:

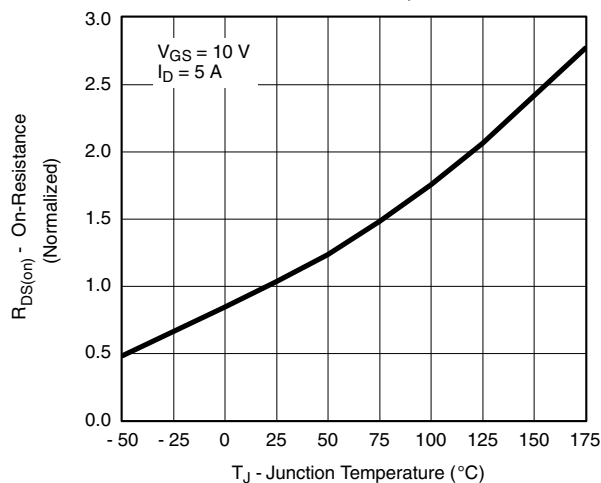
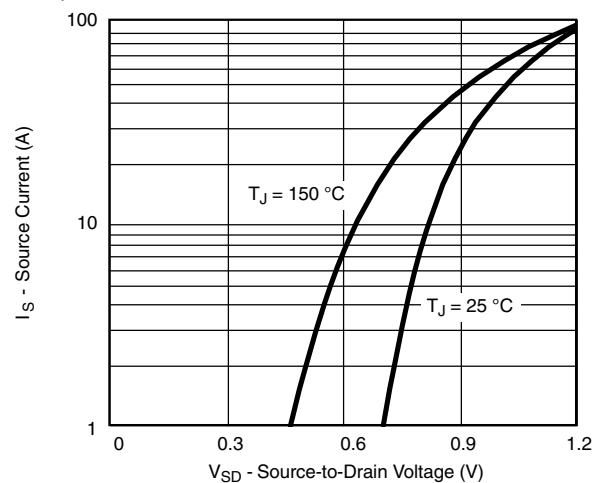
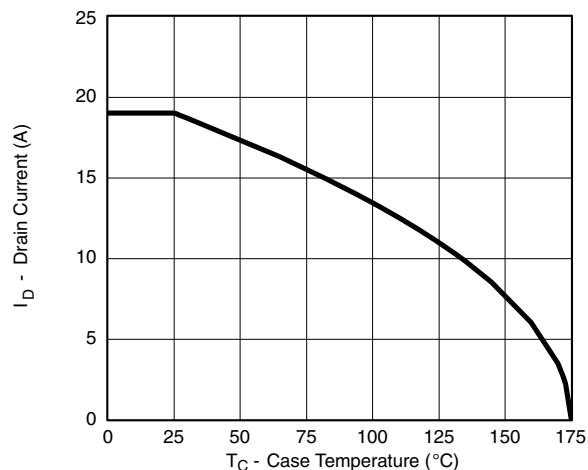
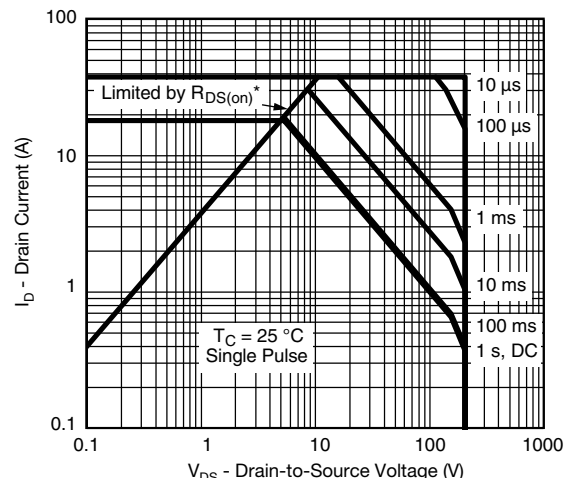
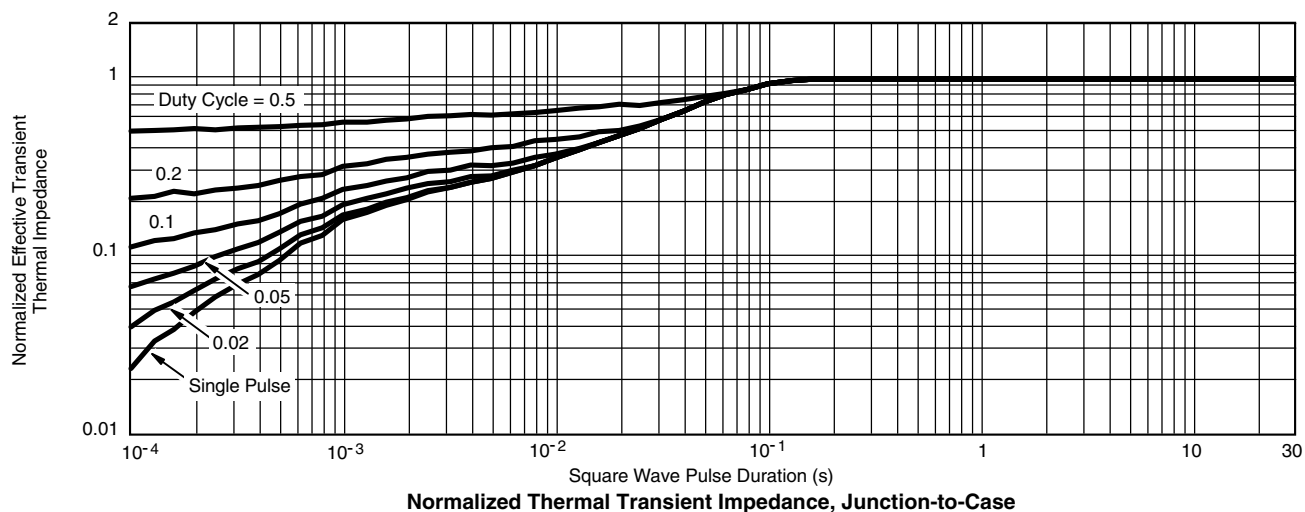
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

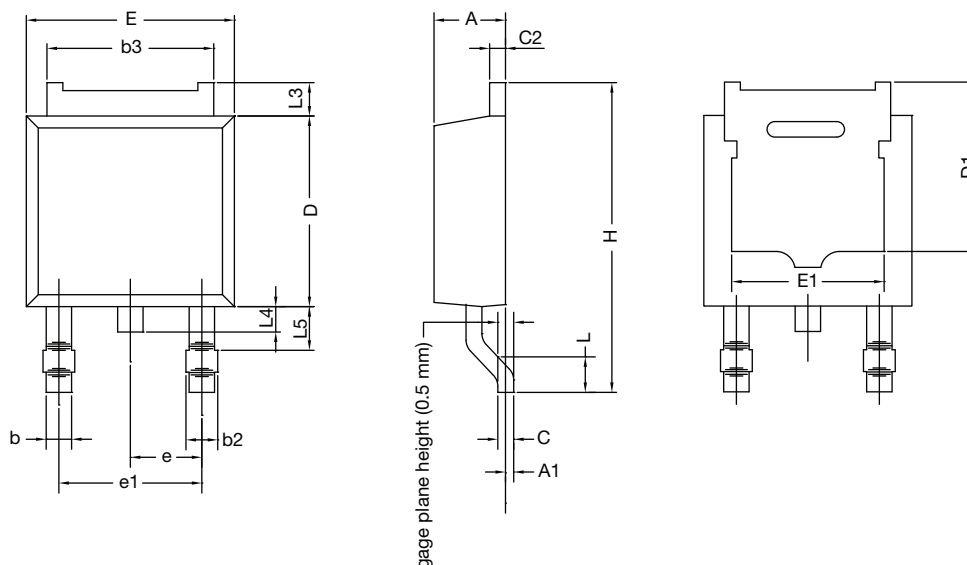
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****THERMAL RATINGS****Maximum Avalanche Drain Current vs. Case Temperature****Safe Operating Area****Normalized Thermal Transient Impedance, Junction-to-Case**

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



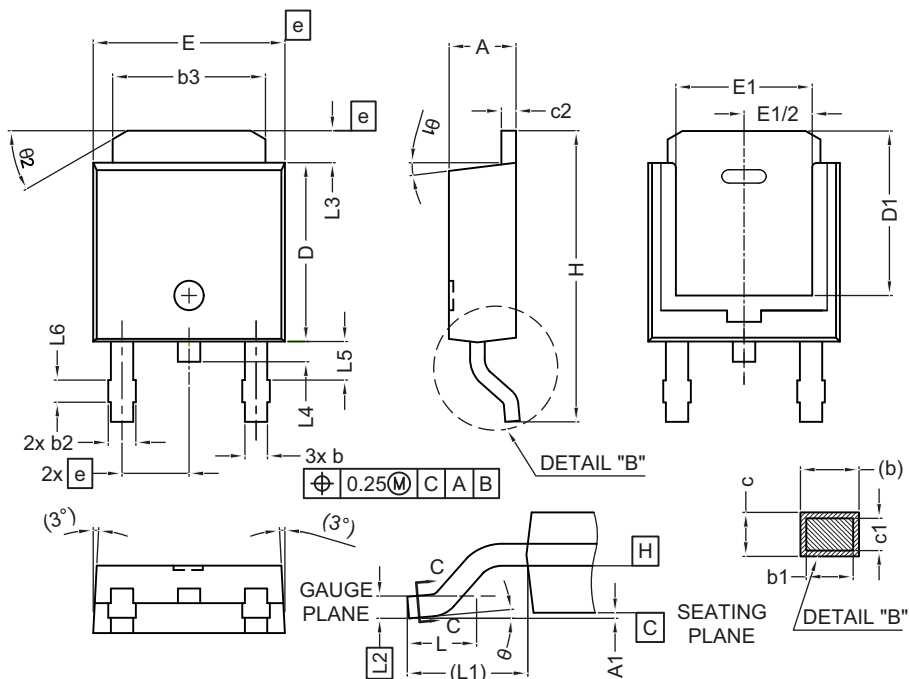
	MILLIMETERS	
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ_1	0°	15°
θ_2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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