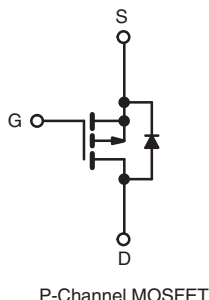
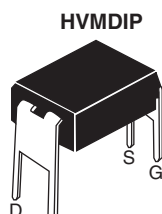


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10$ V	1.5
Q_g (Max.) (nC)	15	
Q_{gs} (nC)	3.2	
Q_{gd} (nC)	8.4	
Configuration	Single	



FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- Fast Switching
- Ease of Paralleling
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Note

* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.



RoHS*
COMPLIANT

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD9220PbF SiHFD9220-E3
SnPb	IRFD9220 SiHFD9220

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	- 200	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_A = 25^\circ\text{C}$	A
		$T_A = 100^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	- 4.5	
Linear Derating Factor		0.0083	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	80	mJ
Avalanche Current ^a	I_{AR}	- 0.56	A
Repetitive Avalanche Energy ^a	E_{AR}	0.10	mJ
Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	W
Peak Diode Recovery dV/dt ^c		dV/dt	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -50$ V, starting $T_J = 25^\circ\text{C}$, $L = 17.8$ mH, $R_g = 25\ \Omega$, $I_{AS} = -3$ A (see fig. 12).
- $I_{SD} \leq -3.9$ A, $dI/dt \leq 95$ A/ μs , $V_{DD} \leq V_{DS}$, $T_J \leq 150^\circ\text{C}$.

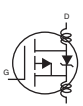


d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = - 1 mA		-	- 0.22	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 200 V, V _{GS} = 0 V		-	-	- 100	μA
		V _{DS} = - 160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	- 500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 0.34 A ^b	-	-	1.5	Ω
Forward Transconductance	g _{fs}	V _{DS} = - 50 V, I _D = - 0.35 A ^b		0.55	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	340	-	pF
Output Capacitance	C _{oss}			-	110	-	
Reverse Transfer Capacitance	C _{rss}			-	33	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 2.1 A, V _{DS} = - 160 V, see fig. 6 and 13 ^b	-	-	15	nC
Gate-Source Charge	Q _{gs}			-	-	3.2	
Gate-Drain Charge	Q _{gd}			-	-	8.4	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 100 V, I _D = - 3.9 A, R _g = 18 Ω, R _D = 24 Ω, see fig. 10 ^b		-	8.8	-	ns
Rise Time	t _r			-	27	-	
Turn-Off Delay Time	t _{d(off)}			-	7.3	-	
Fall Time	t _f			-	19	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 0.56	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 4.5	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 0.56 A, V _{GS} = 0 V ^b		-	-	- 6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 3.9 A, dI/dt = 100 A/μs ^b		-	150	300	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.97	2.0	μC

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

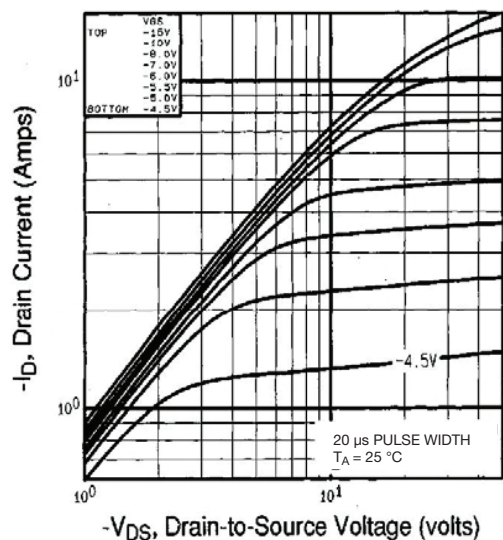


Fig. 1 - Typical Output Characteristics, $T_A = 25\text{ }^{\circ}\text{C}$

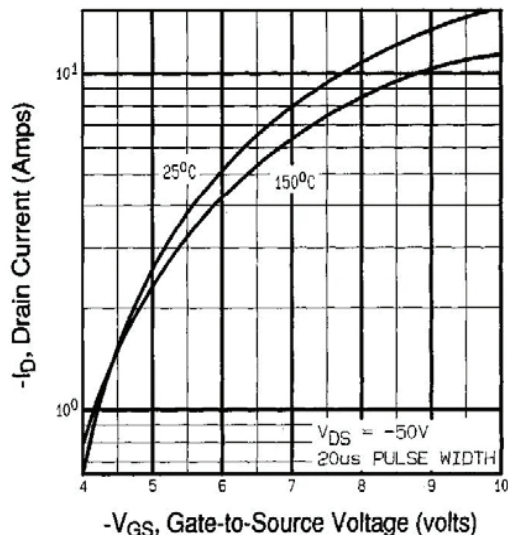


Fig. 3 - Typical Transfer Characteristics

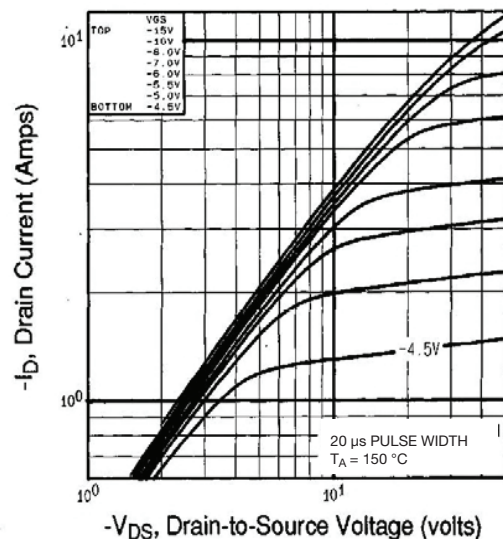


Fig. 2 - Typical Output Characteristics, $T_A = 150\text{ }^{\circ}\text{C}$

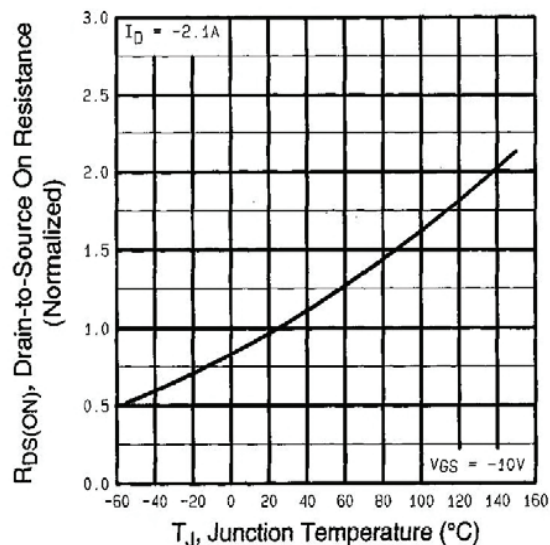


Fig. 4 - Normalized On-Resistance vs. Temperature

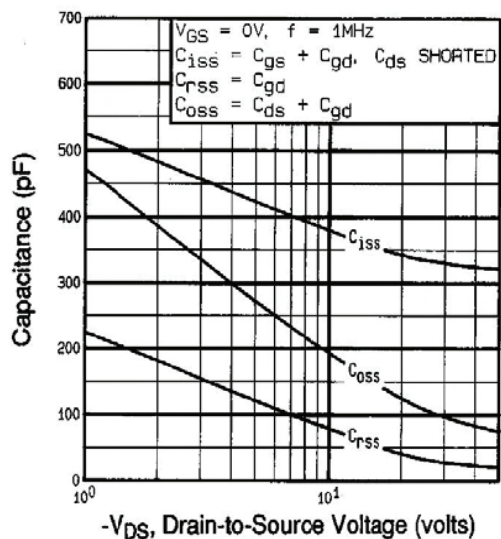


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

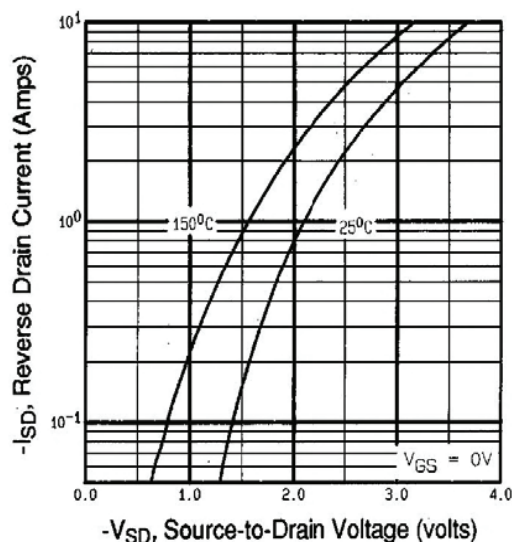


Fig. 7 - Typical Source-Drain Diode Forward Voltage

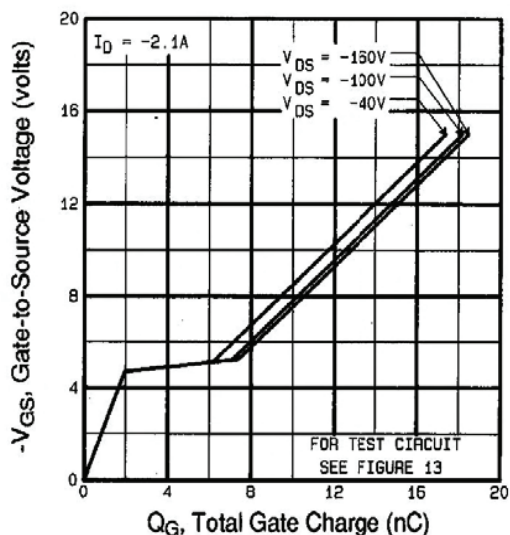


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

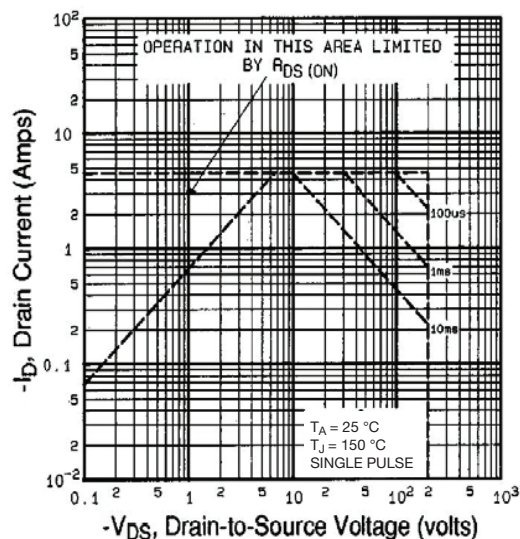
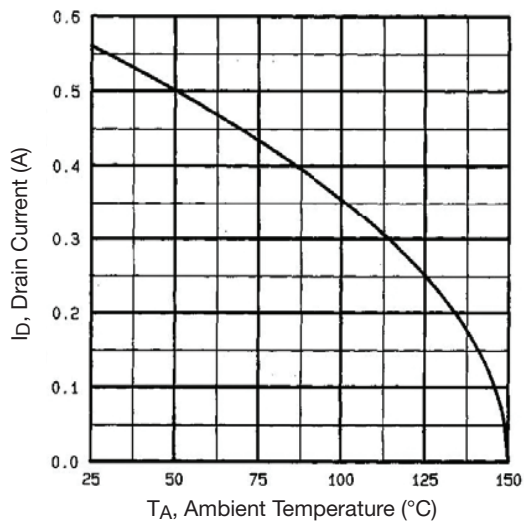
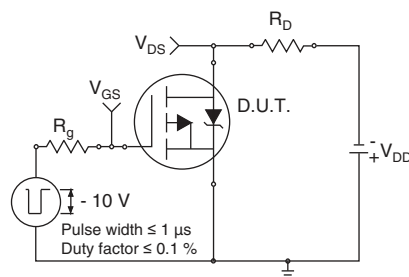
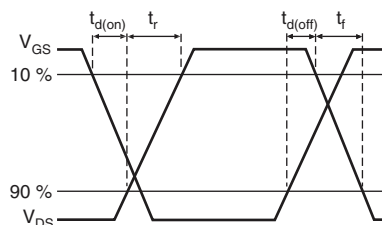
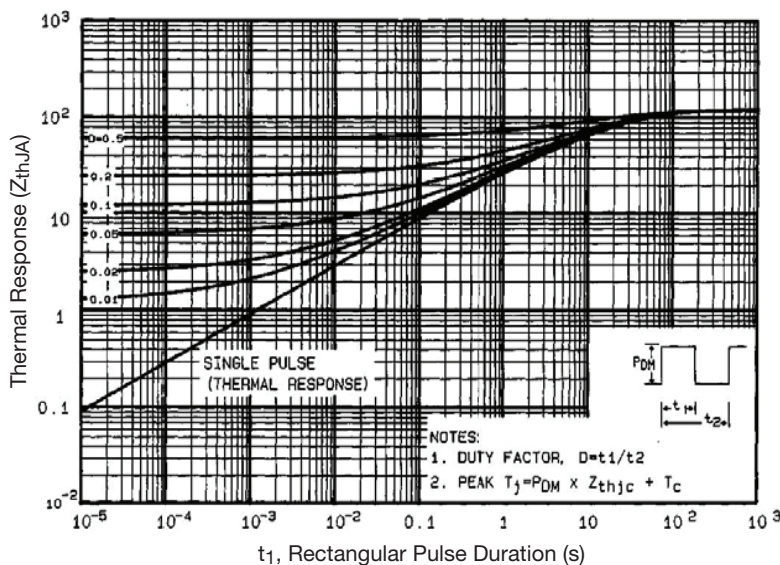
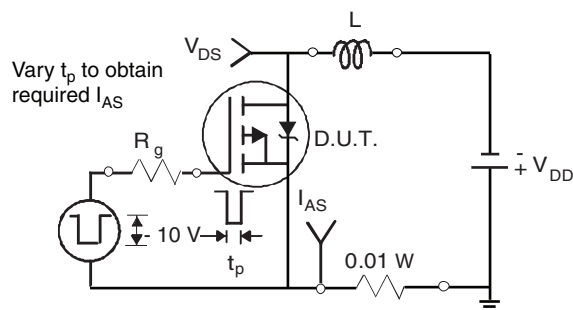
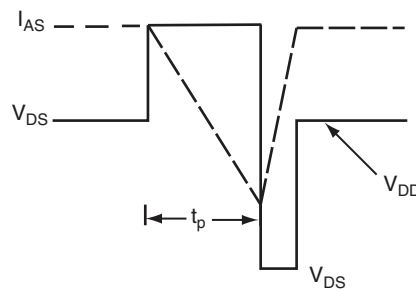
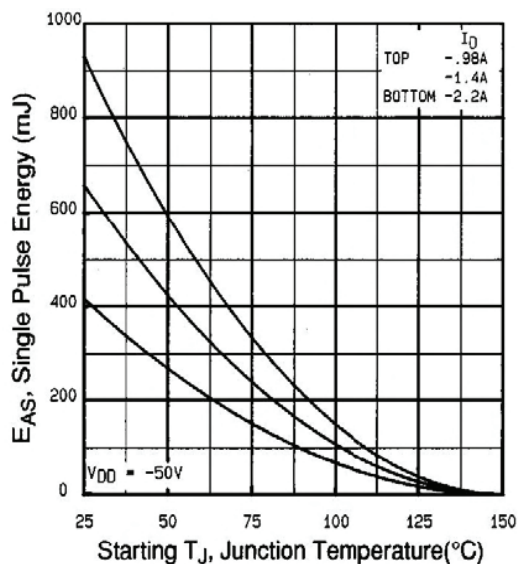
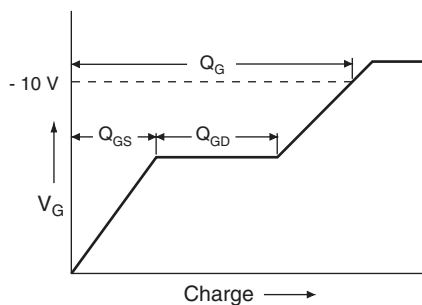
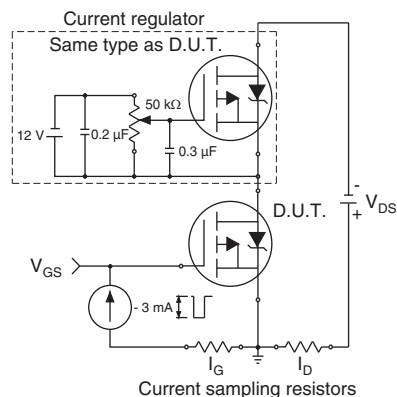


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

Fig. 10 - Switching Time Test Circuit

Fig. 11 - Switching Time Waveforms

Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


Fig. 13 - Unclamped Inductive Test Circuit

Fig. 14 - Unclamped Inductive Waveforms

Fig. 15 - Maximum Avalanche Energy vs. Drain Current

Fig. 16 - Basic Gate Charge Waveform

Fig. 17 - Gate Charge Test Circuit

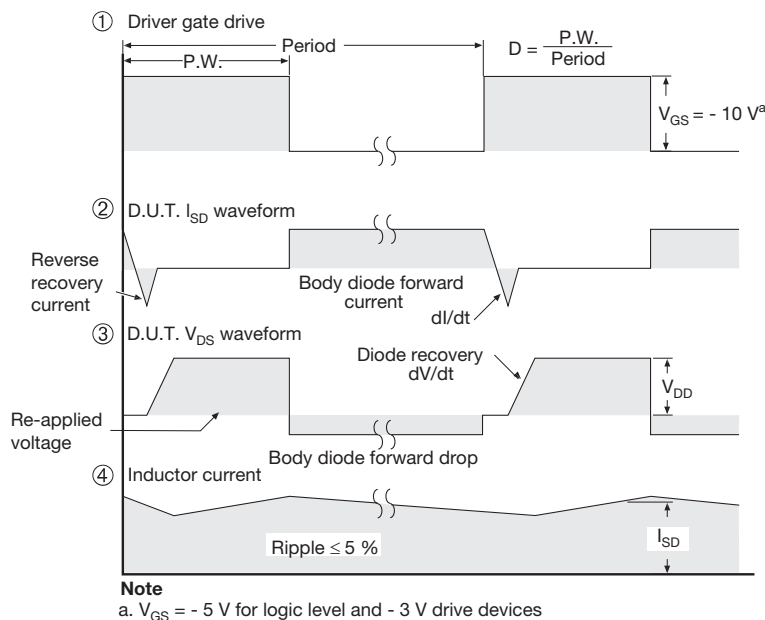
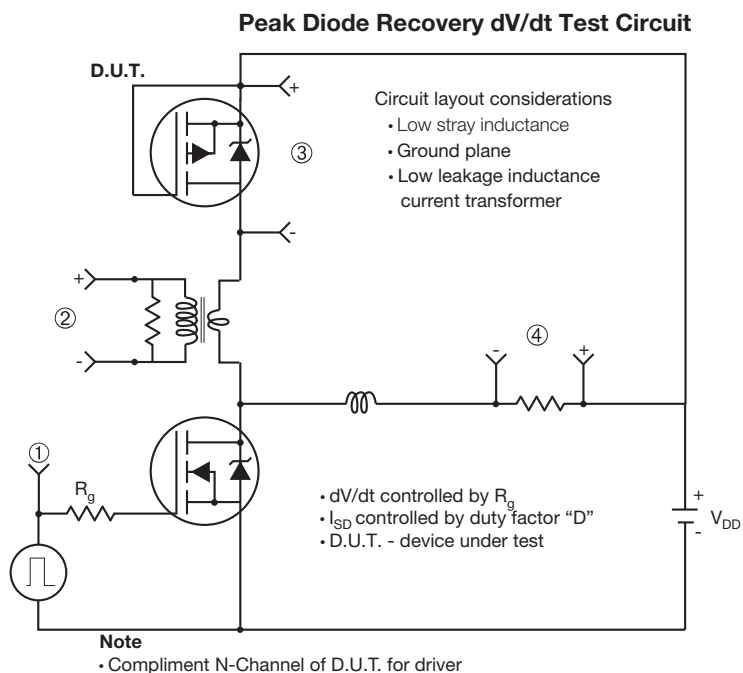
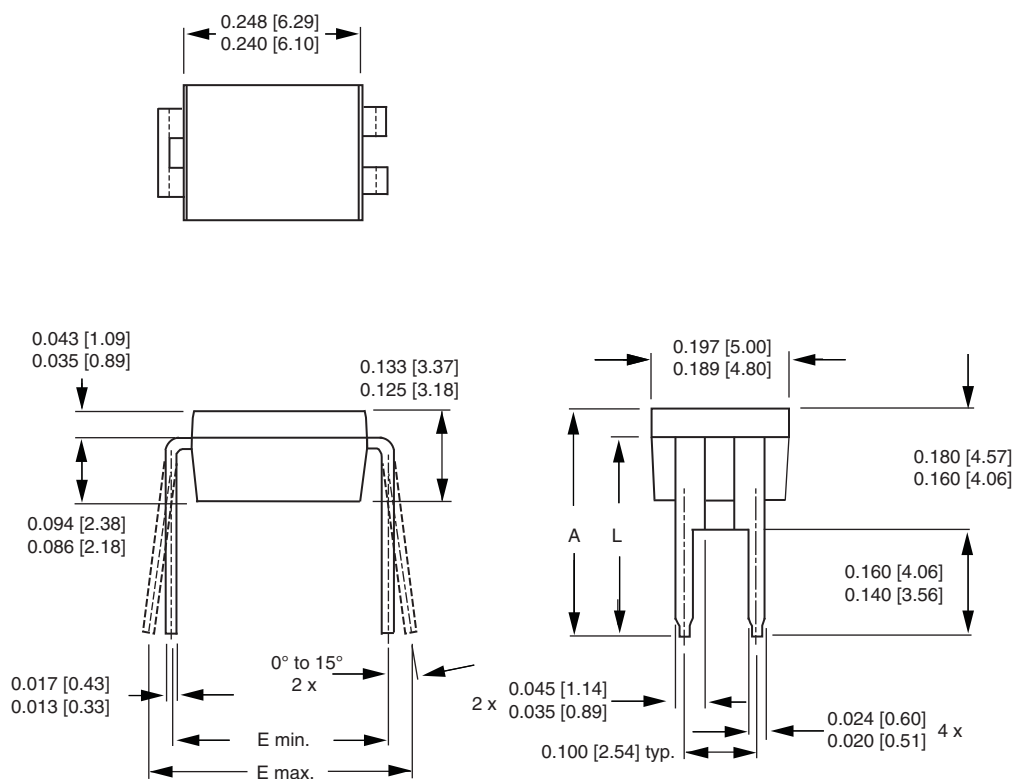


Fig. 18 - For P-Channel

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HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10
DWG: 5974

Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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