

N-channel 500 V, 0.08 Ω typ., 45 A MDmesh™ Power MOSFET in a TO-247 package

Datasheet - production data

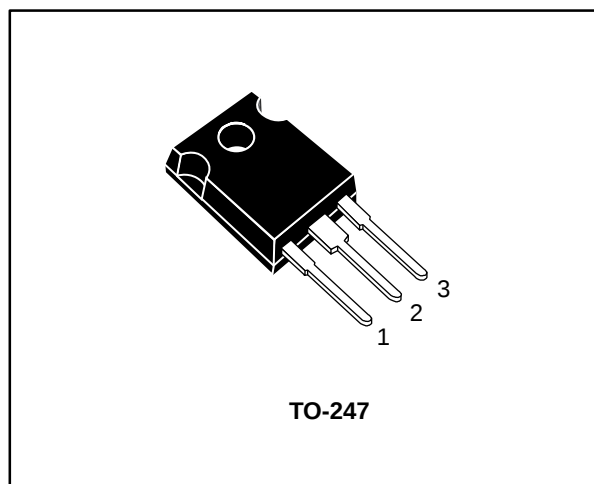
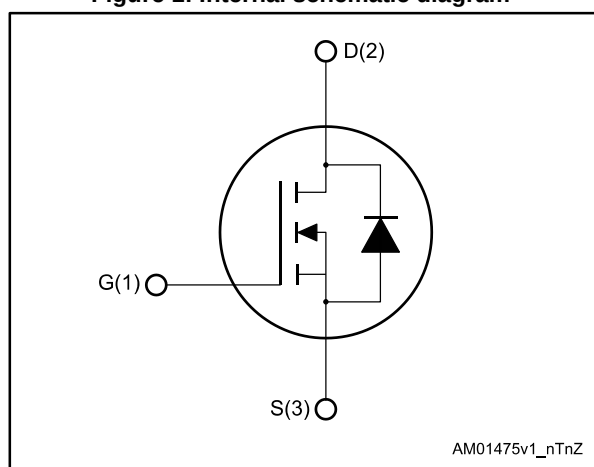


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STW45NM50	500 V	0.1 Ω	45 A

- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using STMicroelectronics' revolutionary MDmesh™ technology, which associates the multiple drain process with the company's PowerMESH™ horizontal layout. This device offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, this Power MOSFET boasts an overall dynamic performance which is superior to similar products on the market.

Table 1: Device summary

Order code	Marking	Package	Packaging
STW45NM50	W45NM50	TO-247	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	8
4	Package information	9
	4.1 TO-247 package information.....	9
5	Revision history	11

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	45	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	28.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	390	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 45\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} \leq V_{(BR)DSS}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.32	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	30	$^{\circ}\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\text{ max}}$)	15	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^{\circ}\text{C}$, $I_D=I_{AR}$, $V_{DD}=50\text{ V}$)	700	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	500			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 500 V			10	μA
		V _{GS} = 0 V, V _{DS} = 500 V, T _C = 125 °C ⁽¹⁾			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±30 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 22.5 A		0.08	0.1	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	3290	-	pF
C _{oss}	Output capacitance		-	865	-	pF
C _{rss}	Reverse transfer capacitance		-	140	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 to 400 V	-	270	-	pF
Q _g	Total gate charge	V _{DD} = 400 V, I _D = 45 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	113	-	nC
Q _{gs}	Gate-source charge		-	17	-	nC
Q _{gd}	Gate-drain charge		-	82	-	nC
R _G	Gate input resistance	f = 1 MHz, I _D = 0 A	-	1.7	-	Ω

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 22.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	29.1	-	ns
t_r	Rise time		-	73.6	-	ns
$t_{r(voff)}$	Off-voltage rise time	$V_{DD} = 400\text{ V}$, $I_D = 45\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	20.8	-	ns
t_f	Fall time		-	58.3	-	ns
t_c	Cross-over time		-	67.6	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 45\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 45\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	454		ns
Q_{rr}	Reverse recovery charge		-	9380		nC
I_{RRM}	Reverse recovery current		-	41.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 45\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	567		ns
Q_{rr}	Reverse recovery charge		-	12700		nC
I_{RRM}	Reverse recovery current		-	44.8		A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

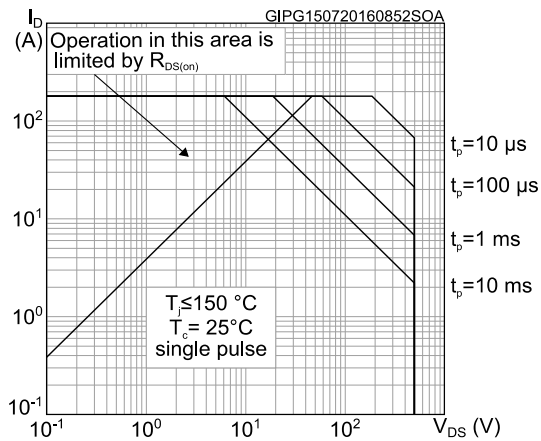


Figure 3: Thermal impedance

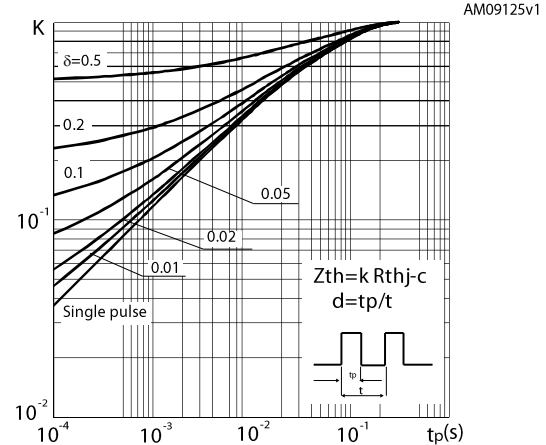


Figure 4: Output characteristics

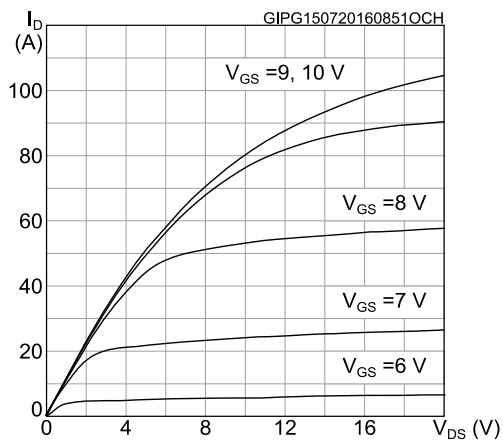


Figure 5: Transfer characteristics

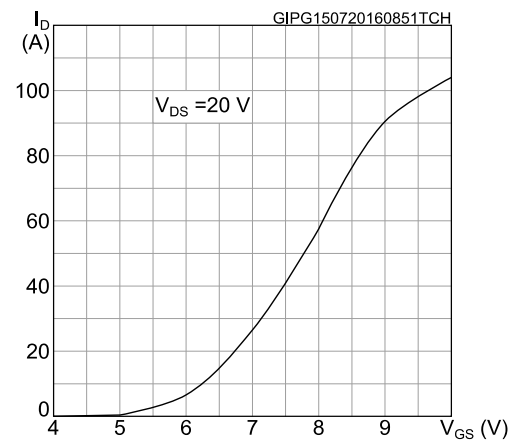


Figure 6: Gate charge vs gate-source voltage

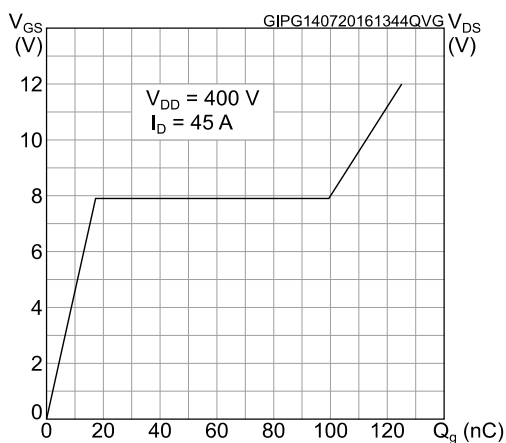


Figure 7: Static drain-source on resistance

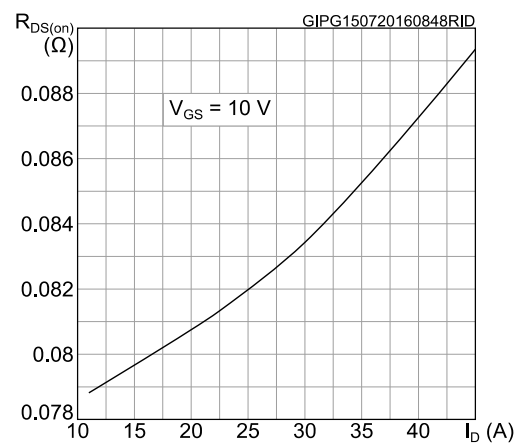


Figure 8: Capacitance variations

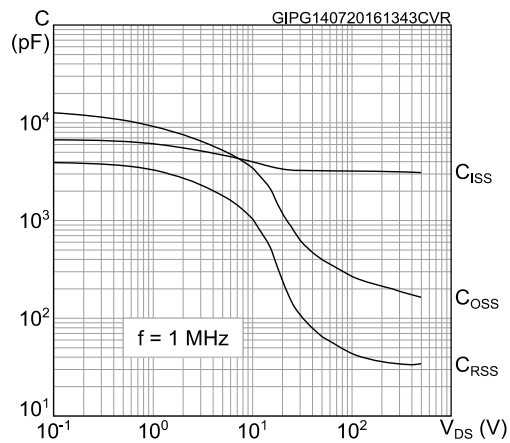


Figure 9: Normalized gate threshold voltage vs temperature

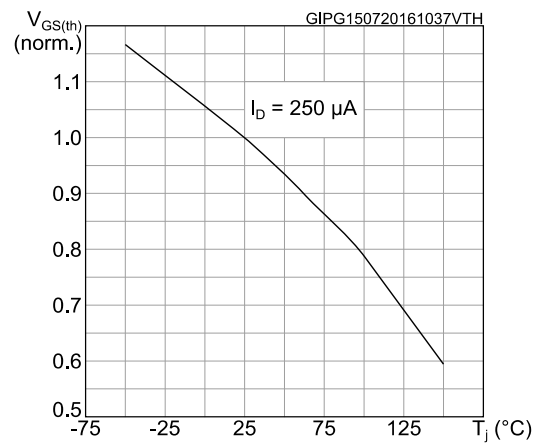


Figure 10: Normalized on-resistance vs temperature

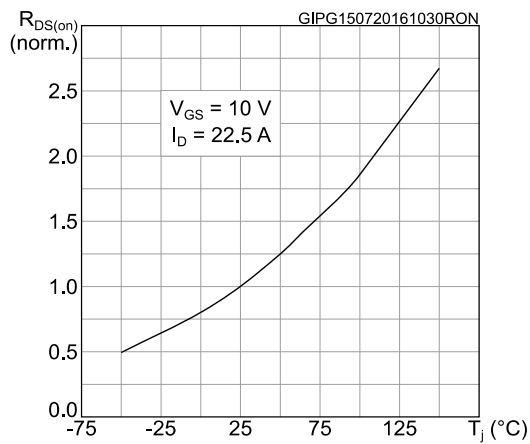


Figure 11: Normalized V(BR)DSS vs temperature

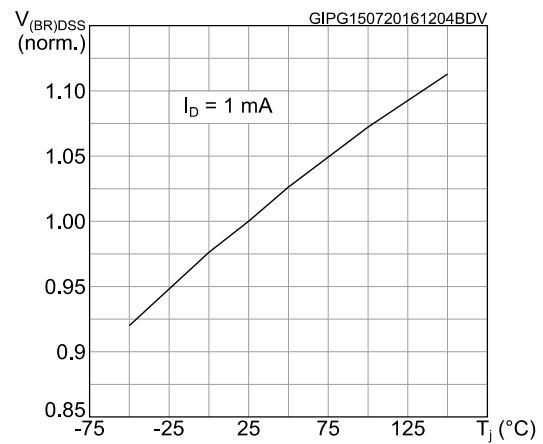
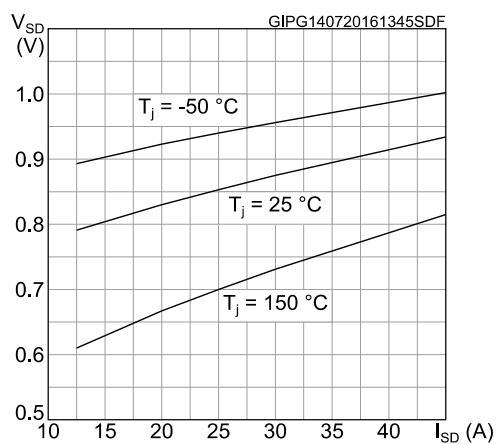
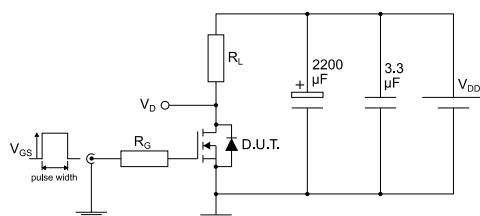


Figure 12: Source-drain diode forward characteristics



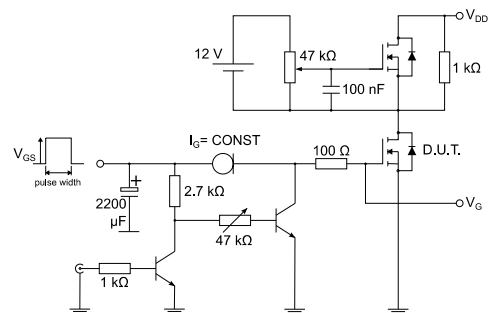
3 Test circuits

Figure 13: Test circuit for resistive load switching times



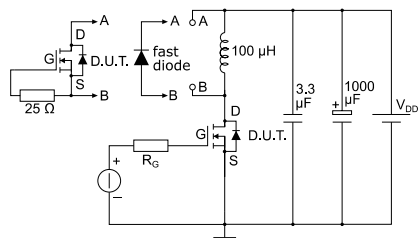
AM01468v1

Figure 14: Test circuit for gate charge behavior



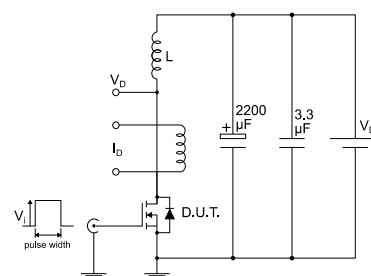
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



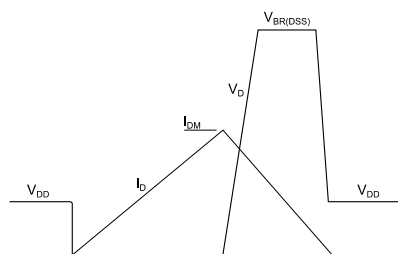
AM01470v1

Figure 16: Unclamped inductive load test circuit



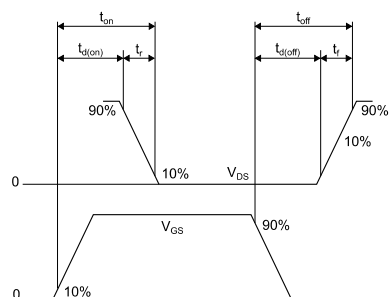
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 19: TO-247 package outline

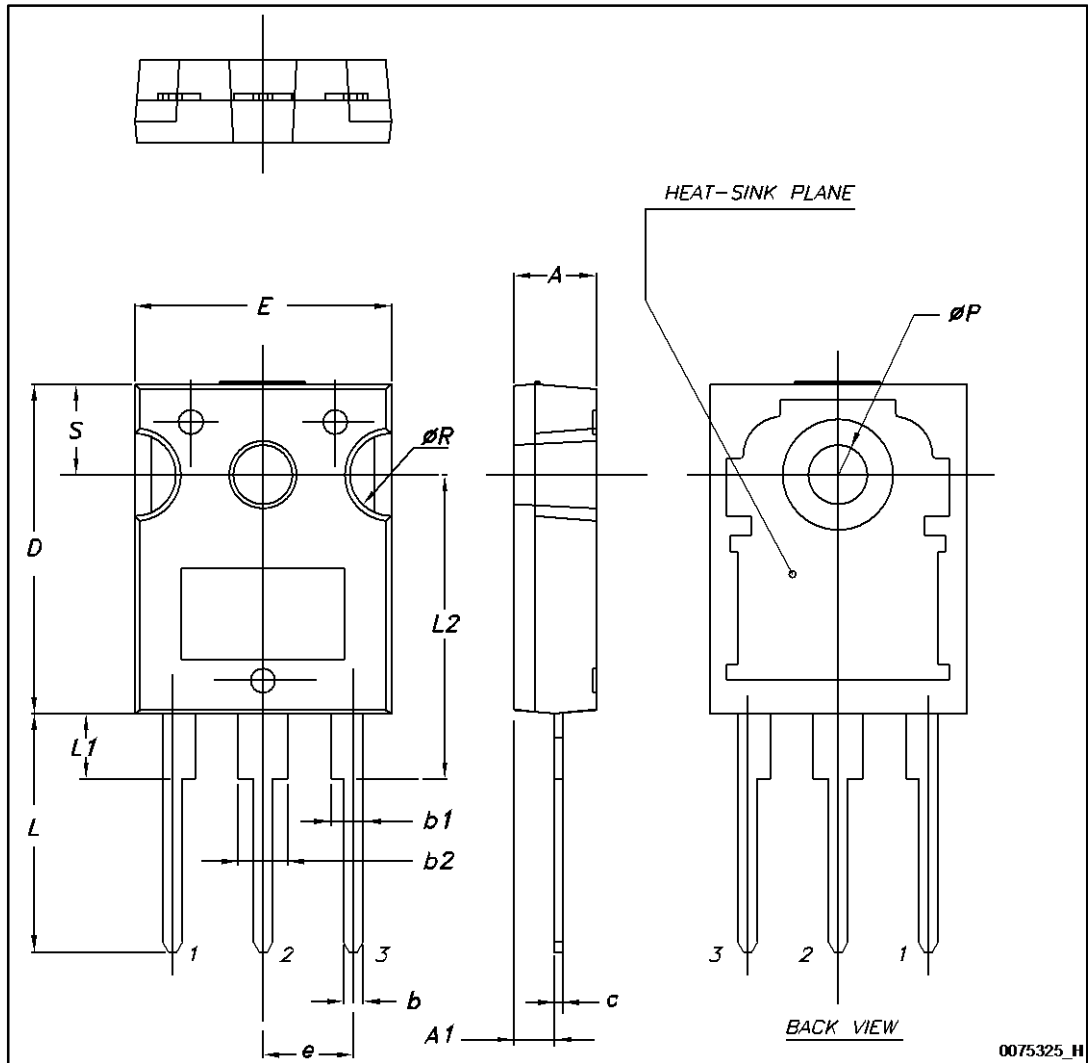


Table 9: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
30-Mar-2005	4	Modified value on <i>Source drain diode</i>
23-Jul-2009	5	Modified values on <i>Switching times</i>
18-Jul-2016	6	Modified: Table 2: "Absolute maximum ratings" , Table 3: "Thermal data" , Table 4: "Avalanche characteristics" , Table 5: "On/off states" , Table 6: "Dynamic" , Table 7: "Switching times" and Table 8: "Source-drain diode" Modified: Section 5.1: "Electrical characteristics (curves)" Updated: Section 7.1: "TO-247 package information"

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved