

DATA SHEET

BF998; BF998R

Silicon N-channel dual-gate
MOS-FETs

Product specification
Supersedes data of April 1991

1996 Aug 01



Silicon N-channel dual-gate MOS-FETs

BF998; BF998R

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz.

APPLICATIONS

- VHF and UHF applications with 12 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Depletion type field effect transistor in a plastic microminiature SOT143B or SOT143R package with source and substrate interconnected. The transistors are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

CAUTION

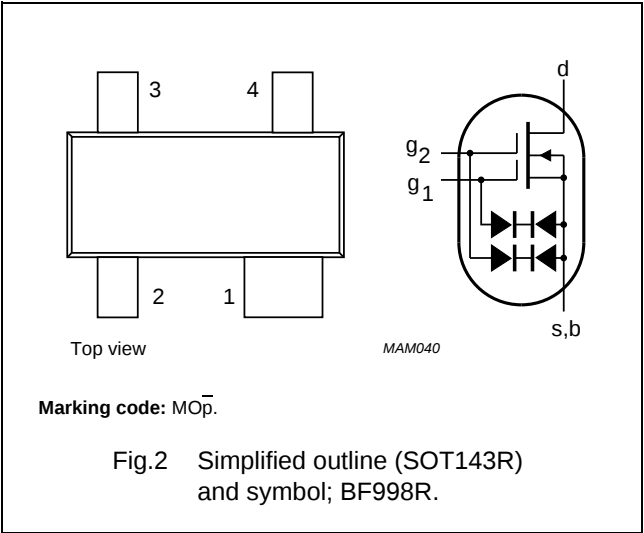
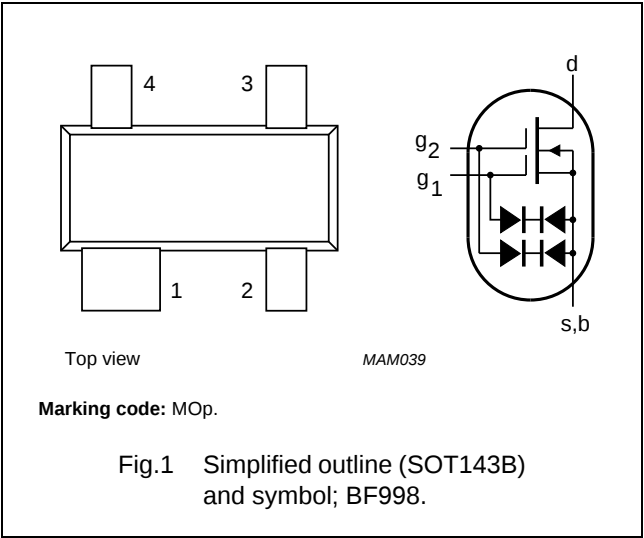
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		–	12	V
I _D	drain current		–	30	mA
P _{tot}	total power dissipation		–	200	mW
y _{fs}	forward transfer admittance		24	–	mS
C _{ig1-s}	input capacitance at gate 1		2.1	–	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	25	–	fF
F	noise figure	f = 800 MHz	1	–	dB
T _j	operating junction temperature		–	150	°C



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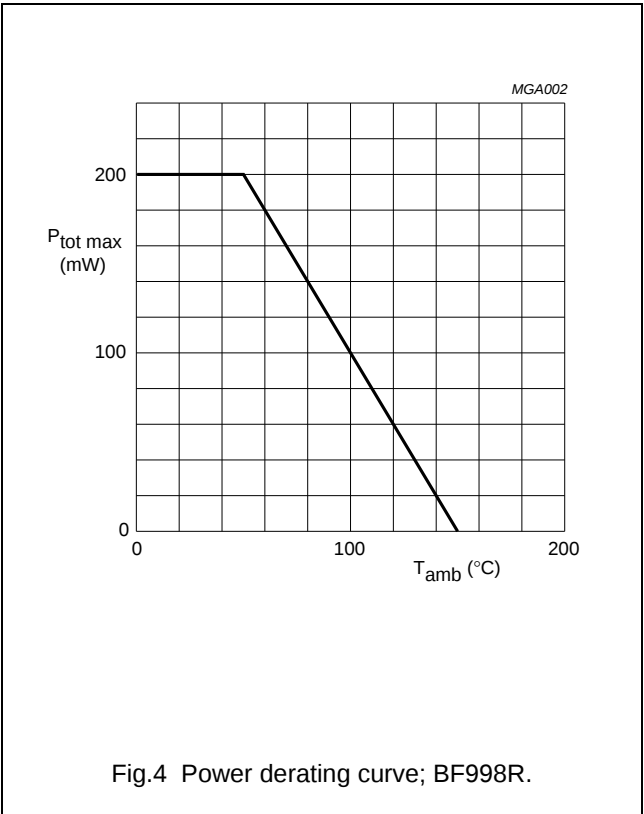
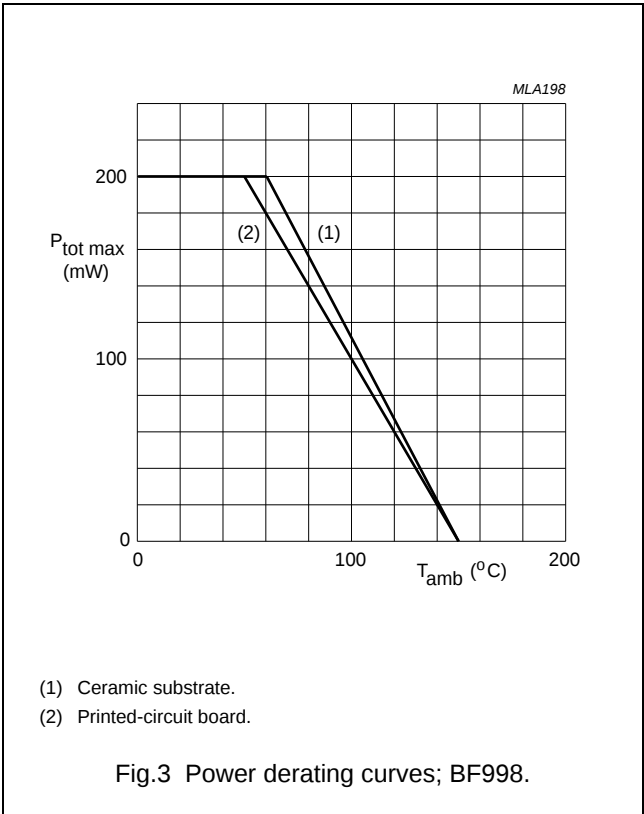
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
I_D	drain current		–	30	mA
$\pm I_{G1}$	gate 1 current		–	10	mA
$\pm I_{G2}$	gate 2 current		–	10	mA
P_{tot}	total power dissipation; BF998	up to $T_{amb} = 60\text{ }^{\circ}\text{C}$; see Fig.3; note 1	–	200	mW
		up to $T_{amb} = 50\text{ }^{\circ}\text{C}$; see Fig.3; note 2	–	200	mW
P_{tot}	total power dissipation; BF998R	up to $T_{amb} = 50\text{ }^{\circ}\text{C}$; see Fig.4; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–	150	$^{\circ}\text{C}$

Notes

- 1. Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
- 2. Device mounted on a printed-circuit board.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air; BF998	note 1	460	K/W
		note 2	500	K/W
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air; BF998R	note 1	500	K/W

Notes

- Device mounted on a ceramic substrate, 8 mm × 10 mm × 0.7 mm.
- Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-SS} = \pm 10\ \text{mA}$	6	20	V
$\pm V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-SS} = \pm 10\ \text{mA}$	6	20	V
$-V_{(P)G1-S}$	gate 1-source cut-off voltage	$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 8\ \text{V}$; $I_D = 20\ \mu\text{A}$	–	2.0	V
$-V_{(P)G2-S}$	gate 2-source cut-off voltage	$V_{G1-S} = 0$; $V_{DS} = 8\ \text{V}$; $I_D = 20\ \mu\text{A}$	–	1.5	V
I_{DSS}	drain-source current	$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 8\ \text{V}$; $V_{G1-S} = 0$; note 1	2	18	mA
$\pm I_{G1-SS}$	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = \pm 5\ \text{V}$	–	50	nA
$\pm I_{G2-SS}$	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = \pm 5\ \text{V}$	–	50	nA

Note

- Measured under pulse condition.

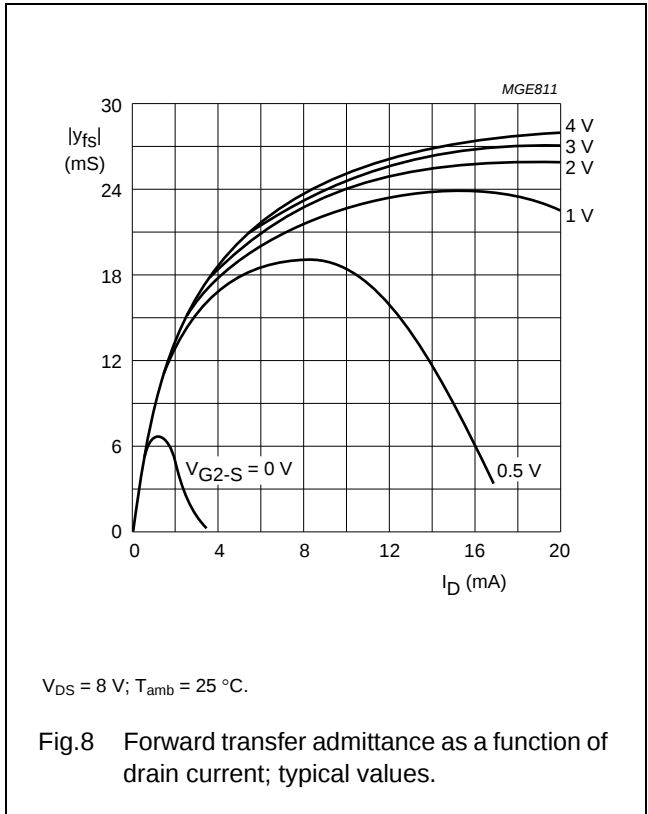
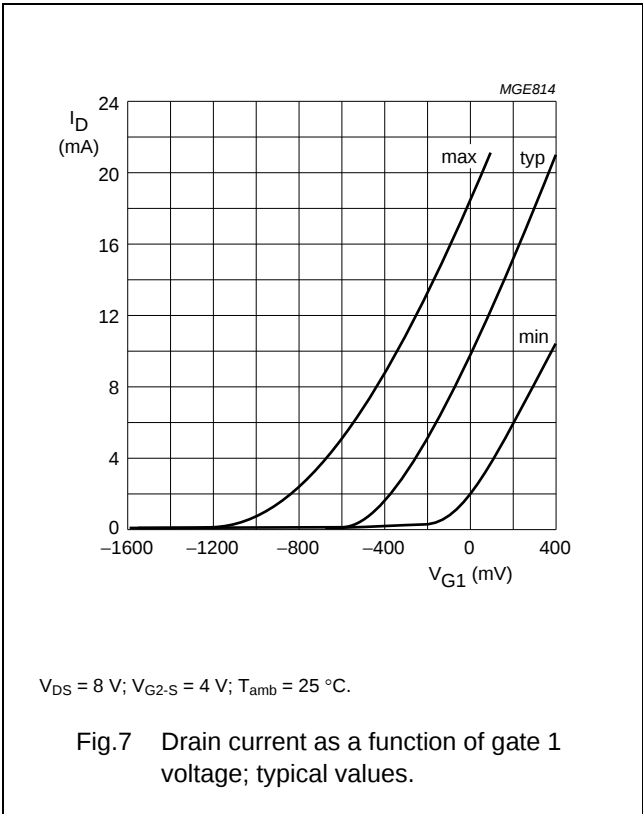
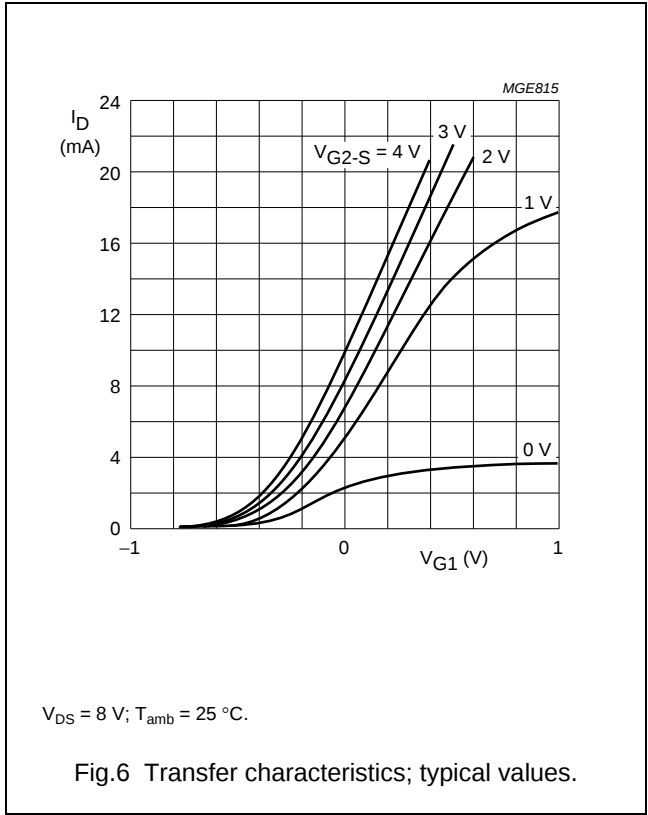
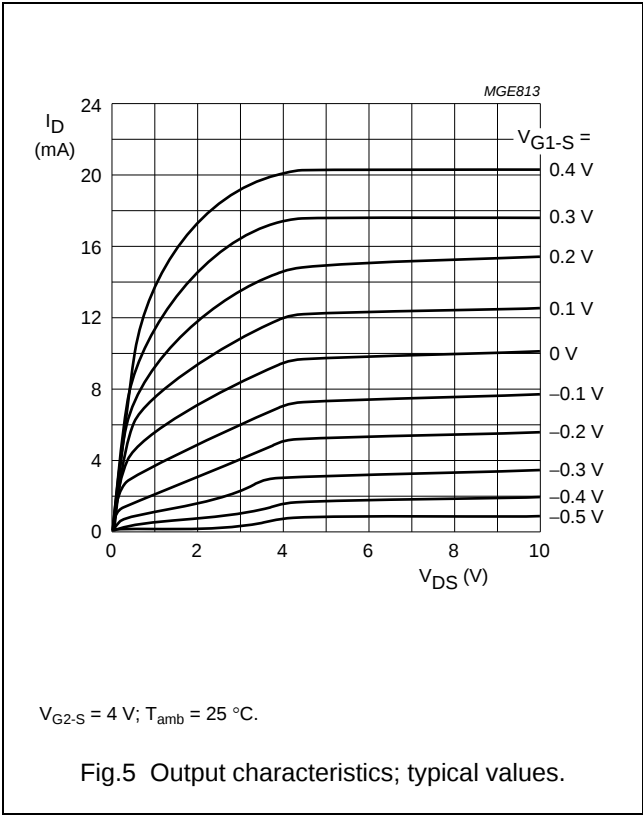
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\ ^\circ\text{C}$; $V_{DS} = 8\ \text{V}$; $V_{G2-S} = 4\ \text{V}$; $I_D = 10\ \text{mA}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	$f = 1\ \text{kHz}$	21	24	–	mS
C_{ig1-s}	input capacitance at gate 1	$f = 1\ \text{MHz}$	–	2.1	2.5	pF
C_{ig2-s}	input capacitance at gate 2	$f = 1\ \text{MHz}$	–	1.2	–	pF
C_{os}	output capacitance	$f = 1\ \text{MHz}$	–	1.05	–	pF
C_{rs}	reverse transfer capacitance	$f = 1\ \text{MHz}$	–	25	–	fF
F	noise figure	$f = 200\ \text{MHz}$; $G_S = 2\ \text{mS}$; $B_S = B_{Sopt}$	–	0.6	–	dB
		$f = 800\ \text{MHz}$; $G_S = 3.3\ \text{mS}$; $B_S = B_{Sopt}$	–	1.0	–	dB

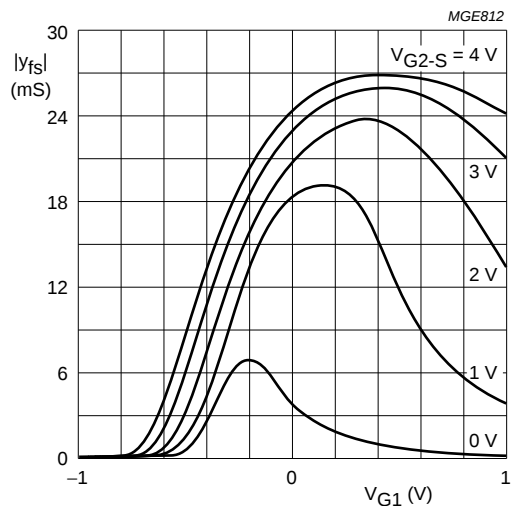
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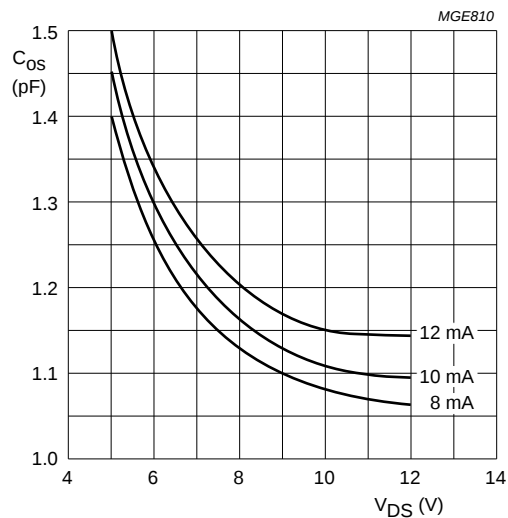
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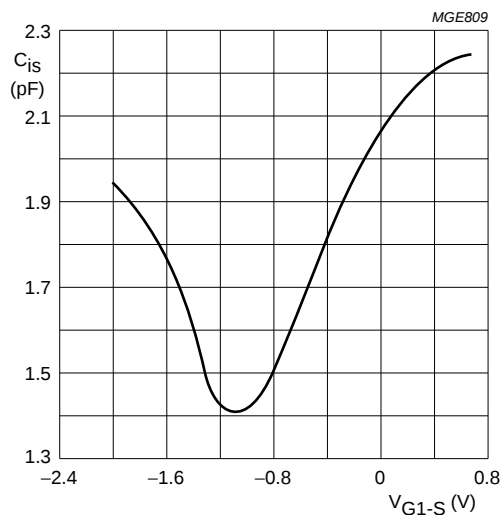
$V_{DS} = 8\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.9 Forward transfer admittance as a function of gate 1 voltage; typical values.



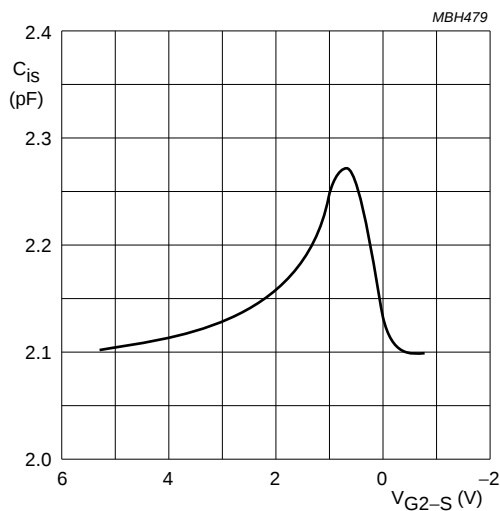
$V_{G2-S} = 4\text{ V}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.10 Output capacitance as a function of drain-source voltage; typical values.



$V_{DS} = 8\text{ V}$; $V_{G2-S} = 4\text{ V}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.11 Gate 1 input capacitance as a function of gate 1-source voltage; typical values.

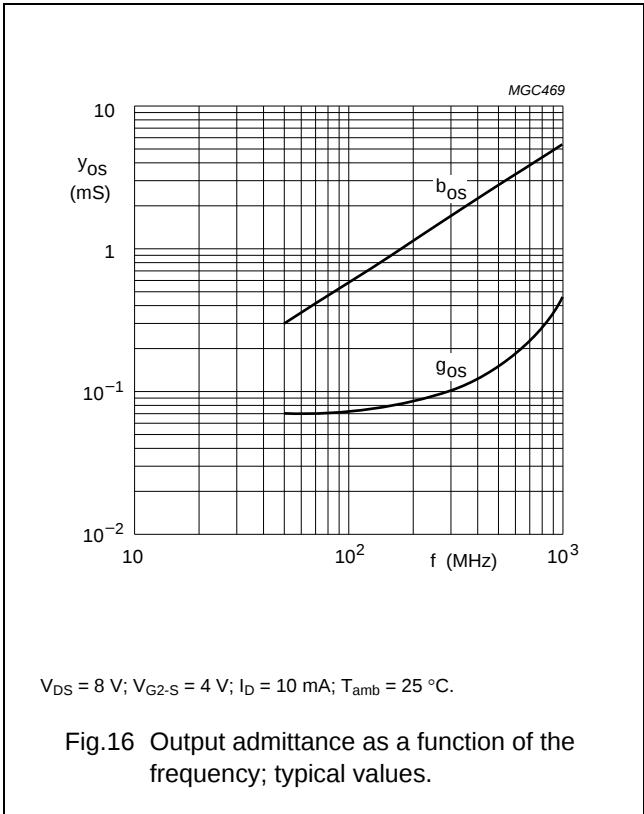
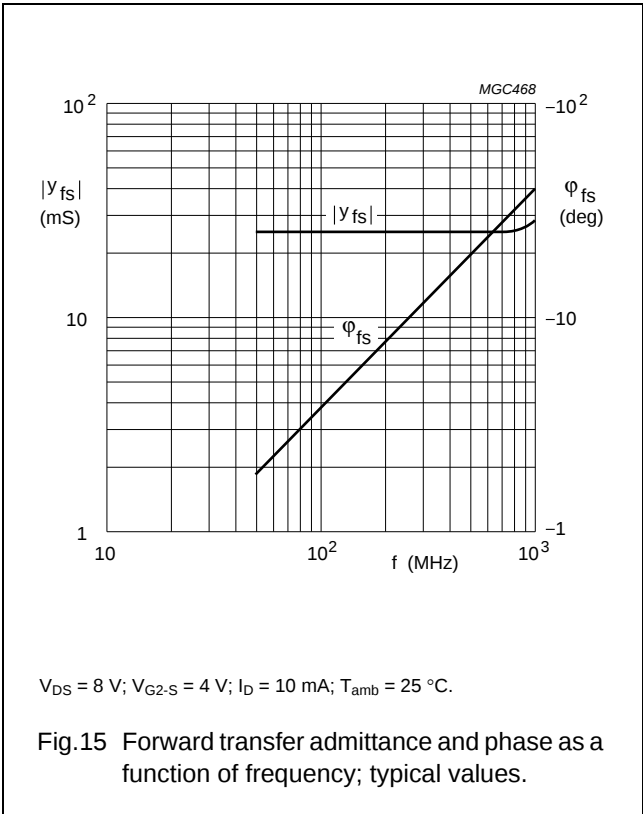
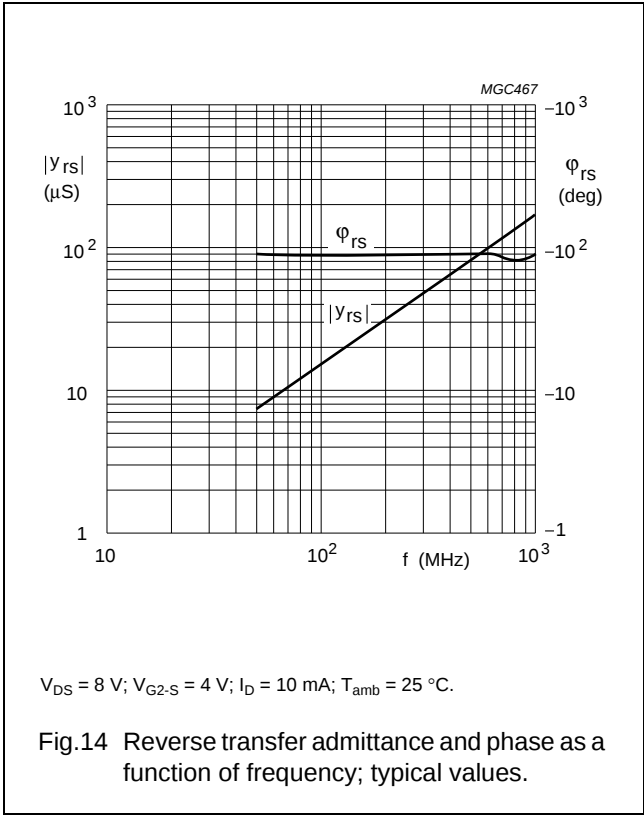
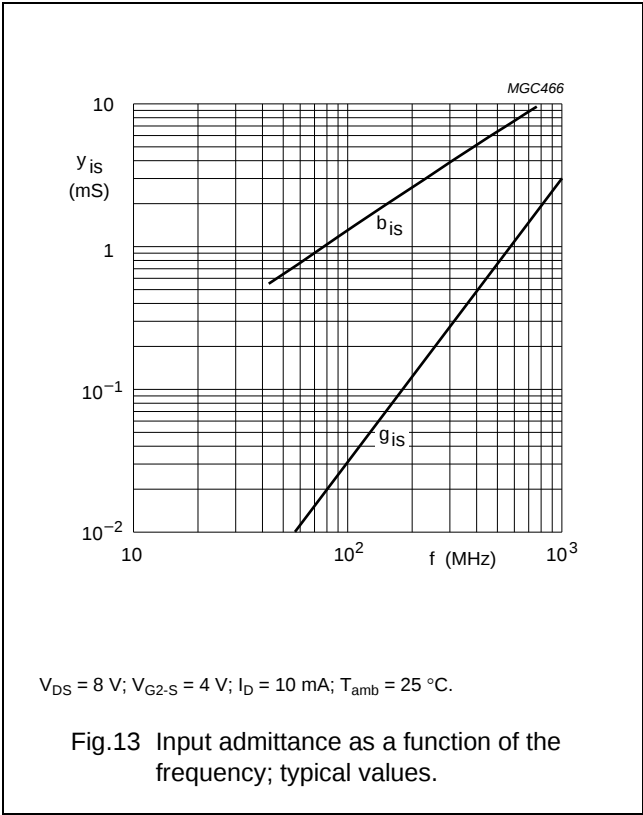


$V_{DS} = 8\text{ V}$; $V_{G1-S} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.12 Gate 1 input capacitance as a function of gate 2-source voltage; typical values.

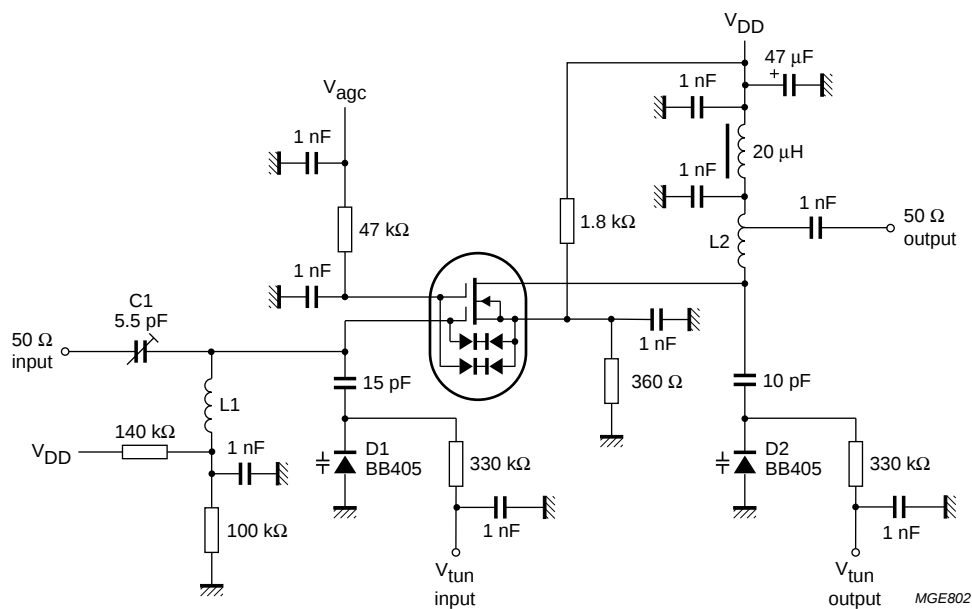
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$$V_{DD} = 12 \text{ V}; G_S = 2 \text{ mS}; G_L = 0.5 \text{ mS}.$$

L1 = 45 nH; 4 turns 0.8 mm copper wire, internal diameter 4 mm.

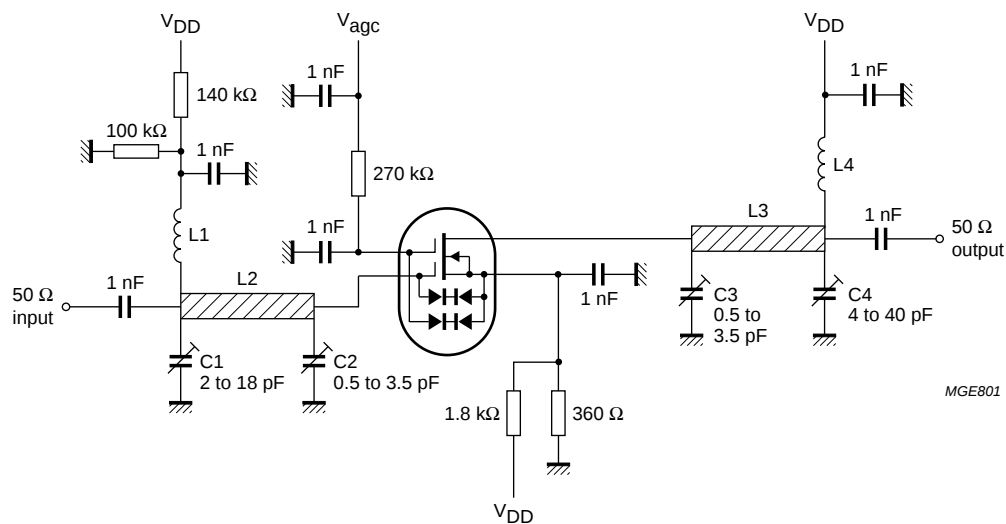
L2 = 160 nH; 3 turns 0.8 mm copper wire, internal diameter 8 mm.

Tapped at approximately half a turn from the cold side, to adjust $G_L = 0.5 \text{ mS}$. C1 adjusted for $G_S = 2 \text{ mS}$.

Fig.17 Gain control test circuit at $f = 200$ MHz.

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$V_{DD} = 12\text{ V}$; $G_S = 3.3\text{ mS}$; $G_L = 1\text{ mS}$.

$L1 = L4 = 200\text{ nH}$; 11 turns 0.5 mm copper wire, without spacing, internal diameter 3 mm.

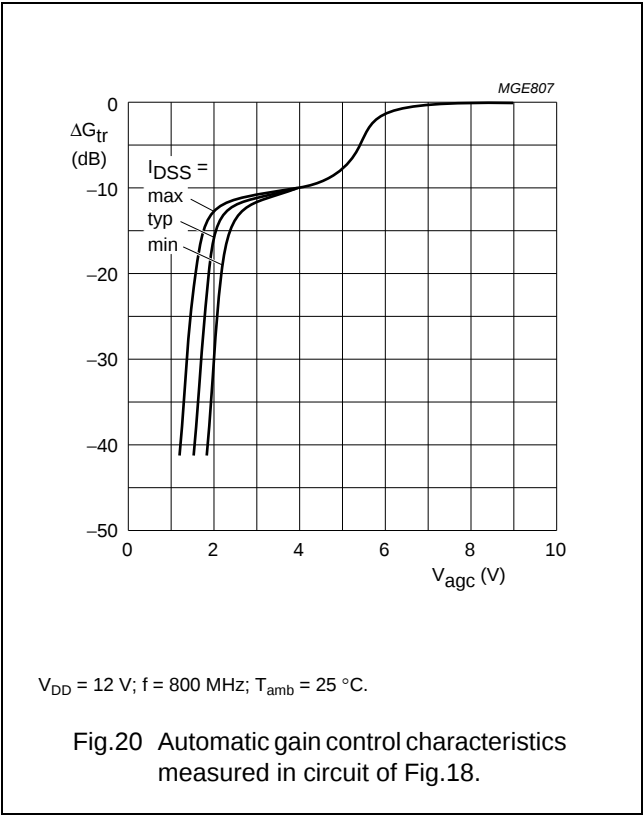
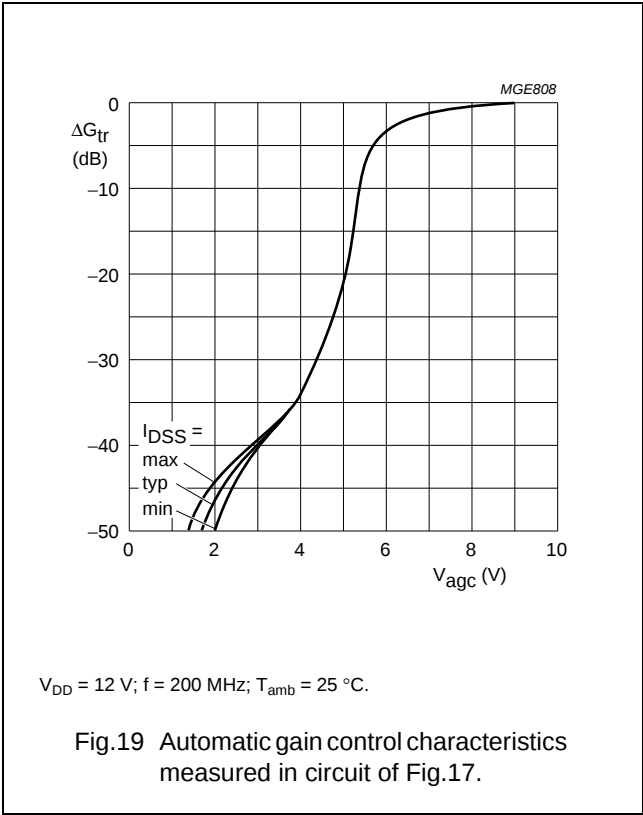
$L2 = 2\text{ cm}$, silvered 0.8 mm copper wire, 4 mm above ground plane.

$L3 = 2\text{ cm}$, silvered 0.5 mm copper wire, 4 mm above ground plane.

Fig.18 Gain control test circuit at $f = 800\text{ MHz}$.

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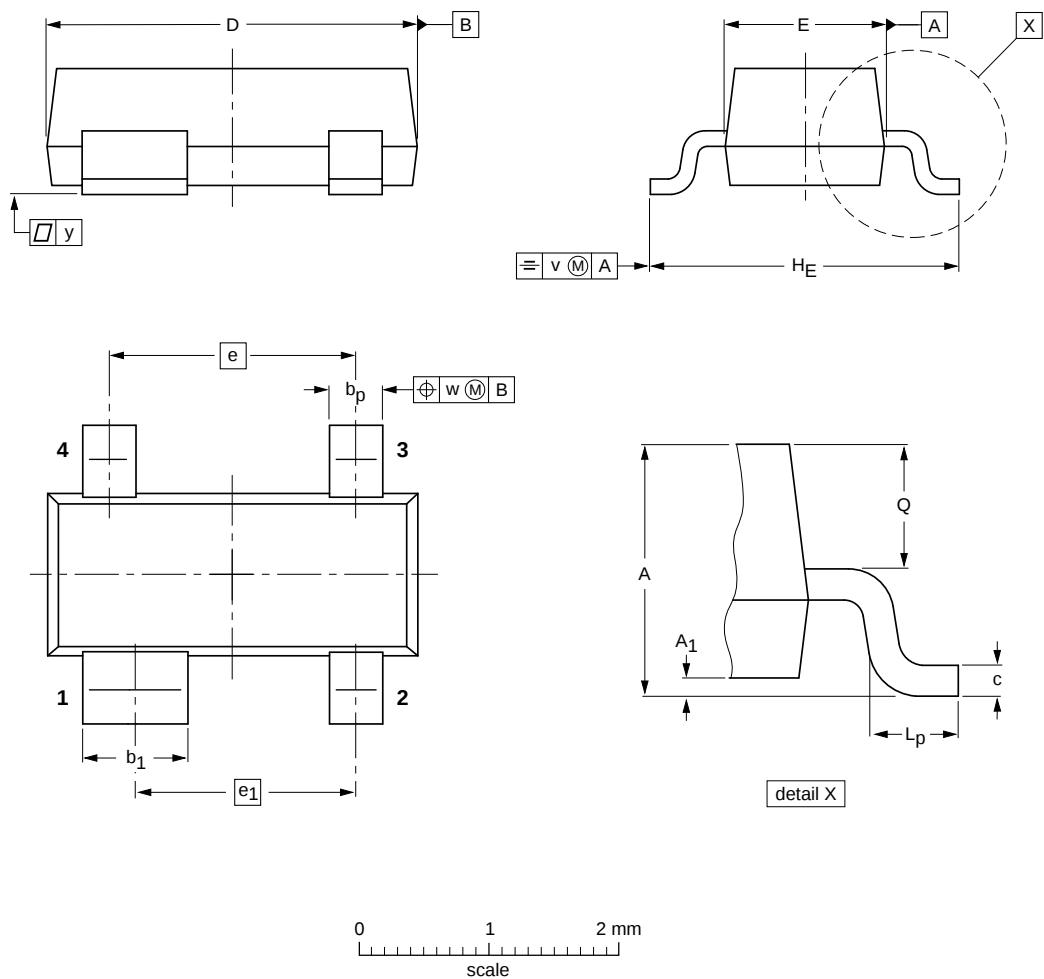
Silicon N-channel dual-gate MOS-FETs

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PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

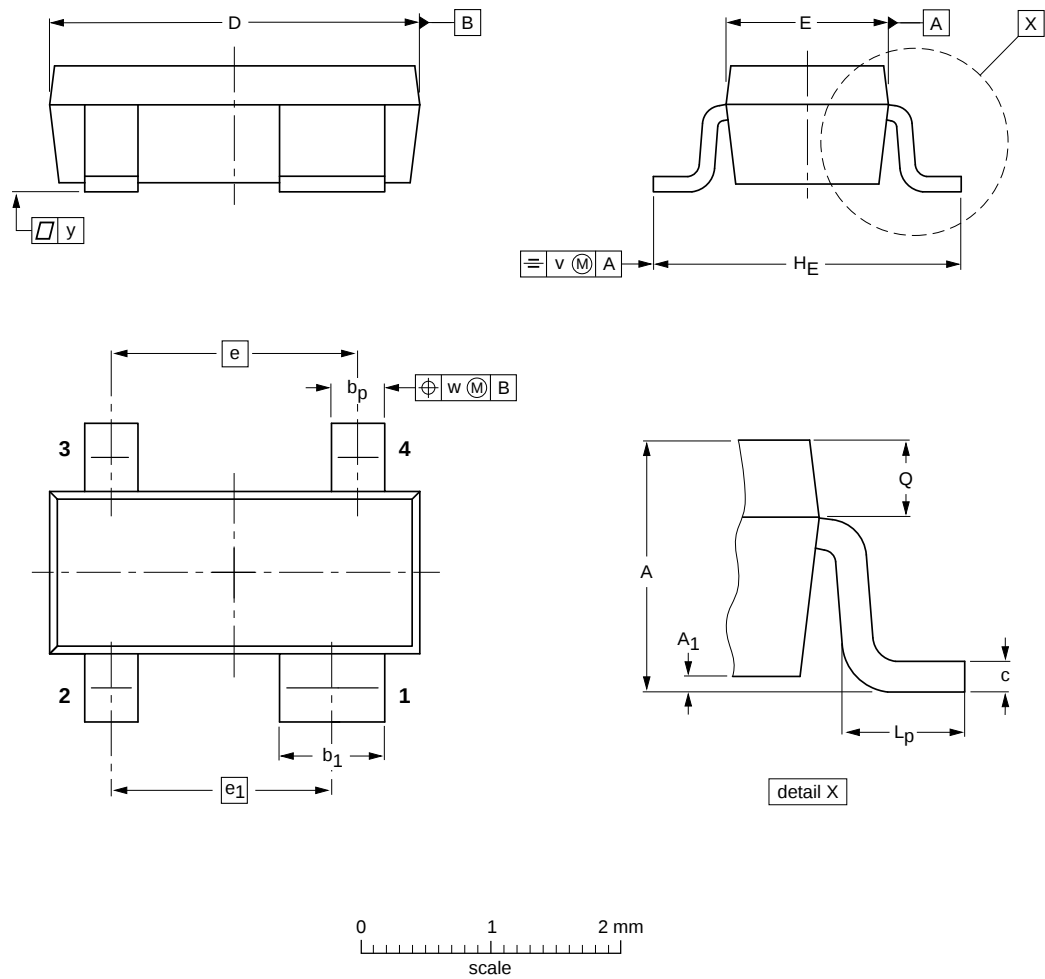
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						04-11-16 06-03-16

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Plastic surface-mounted package; reverse pinning; 4 leads

SOT143R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143R			SC-61AA			04-11-16 06-03-16

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DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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Printed in The Netherlands

R77/02/pp15

Date of release: 1996 Aug 01